PHASE CHANGE MEMORY: ARRAY DEVELOPMENT AND SENSING CIRCUITS USING DELTA-SIGMA MODULATION

by

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DEFENSE COMMITTEE AND FINAL READING APPROVALS

of the thesis submitted by

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The following individuals read and discussed the thesis submitted by student Mahesh Balasubramanian, and they evaluated his presentation and response to questions during the final oral examination. They found that the student passed the final oral examination.

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DEFENSE COMMITTEE APPROVAL

of the Thesis submitted by

Mahesh Balasubramanian

We have read and discussed the Thesis submitted by student Mahesh Balasubramanian, and we have also evaluated his presentation and response to questions during the final oral examination. We find that the student has passed the final oral examination, and that the Thesis is satisfactory for a master's degree and ready for any final modifications that we may explicitly require.

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To the Graduate College of Boise State University:

I have read the Thesis of Mahesh Balasubramanian in its final form and have found that (1) the modifications required by the defense committee are complete; (2) the format, citations, and bibliographic style are consistent and acceptable; (3) the illustrative materials including figures, tables, and charts are in place; and (4) the final manuscript is ready for submission to the Graduate College.

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DEDICATION

This research is dedicated to my parents B. Radha, K. S. Balasubramanian, and my brother and his family for their love, support and encouragement. To all the teachers I had for making me who I am today and to Lord Ganesh for all his blessings.

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ABSTRACT

Chalcogenide based non-volatile Phase Change Memory (PCM) circuits were designed to investigate new emerging non-volatile memory technologies. An overview of the operation of chalcogenide-based resistive PCM for circuit designers is presented. MOSIS fabrication service was used along with Idaho Microfabrication Lab at Boise State University to develop PCM chips. Experimental results show successful integration of two discreet processing services for developing chalcogenide based non-volatile memory circuits. Possible multi-state capabilities were observed during the testing of single memory bits.

Four Delta Sigma Modulation (DSM) based sensing techniques for resistive memory are presented. The proposed sensing techniques have the advantage over traditional sensing circuits in being able to reliably and accurately distinguish resistance values separated by a small margin, easily within 10 kΩ for practical sense times. The experimental results show that resistances varying from 10 kΩ to 4.1 MΩ could be sensed reliably within an error percentage of 15%.

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CHAPTER 1: INTRODUCTION

Phase Change Memory

Memories are widely used in electronic devices for data storage including cellular phones, digital cameras, and portable storage media. Memory technology is mainly classified into volatile and Non Volatile Memory (NVM). Existing volatile memory technology like Dynamic Random Access Memory (DRAM) which works on the principle of charge sharing suffers from scaling limitations, loss of data with the removal of power (volatility) and data corruption due to radiation effects. NVM technology like flash memory which also works on the concept of charge storage, though non volatile, still suffers from scaling limitations and data corruption due to radiation effects. Phase Change Memory (PCM) is a non volatile memory technology and is considered to be one of the most promising candidates for the next generation of memory [1]. The aerospace community considers chalcogenide-based phase-change memory as a likely candidate for non volatile memory for space applications because of its resistance to radiation effects. The apparent limitations of DRAM and flash technology which led to development of PCM are explained in more detail in the following discussion below.

The flash cell shown in Figure 1.1 works on the principle of FNT (Fowler-Nordheim Tunneling). The state of the memory cell is decided based on the charge stored on the floating gate of the flash cell. A cell with electrons trapped in the floating gate due

to FNT acts as a programmed cell and one without any electron is in erased state. To program a cell, high voltage is applied to the control gate attracting electrons to the floating gate. The stored electron causes an increase in the threshold voltage of the flash cell causing the current flowing through the device to decrease for a given gate voltage. When a pre charged bitline is connected to this flash cell, the charge on the bitline does not discharge due to the reduced current flow through the cell. This phenomenon is used in the sensing operation of a flash cell. Since the operation of a Flash memory depends on charge, exposure to radiation has a pronounced effect on its operation. Radiation changes the charge distribution on a flash memory array thus causing unintentional programming or erasing. Flash memory, in addition, also has reliability issues due to its limited number of program/erase cycles. The oxide trapped charges shown in Figure 1.1, due to the repeated program/erase cycles causes the threshold voltages of programmed and erased state to move closer. Thus, to sense a flash cell, a high precision sense-amplifier is required to differentiate between the two narrowly separated states of a Flash cell. This becomes even more important in Multi Level flash Cells (MLC).

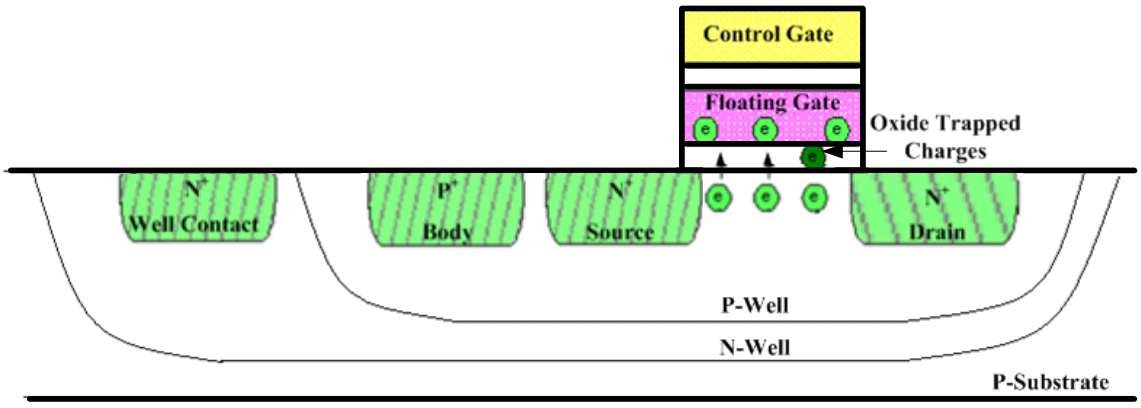


Figure 1.1 A floating gate MOSFET used in a flash cell.

A 1T-1C DRAM architecture shown in Figure 1.2 works on the principle of charge sharing between a pre-charged bitline and the cell capacitance formed between the gate and source of the cell transistor. A DRAM cell is set to be in a programmed/erased state based on the charge stored on the capacitor C_{mbit}. Thus, similar to a Flash cell, exposure to radiation causes an unwanted change in the charge stored both in the bitline capacitance and in the cell capacitance C_{mbit}. In addition to this, a DRAM cell also suffers from loss of data due to charge leakage from C_{mbit} to the bitline and is thus volatile in nature.

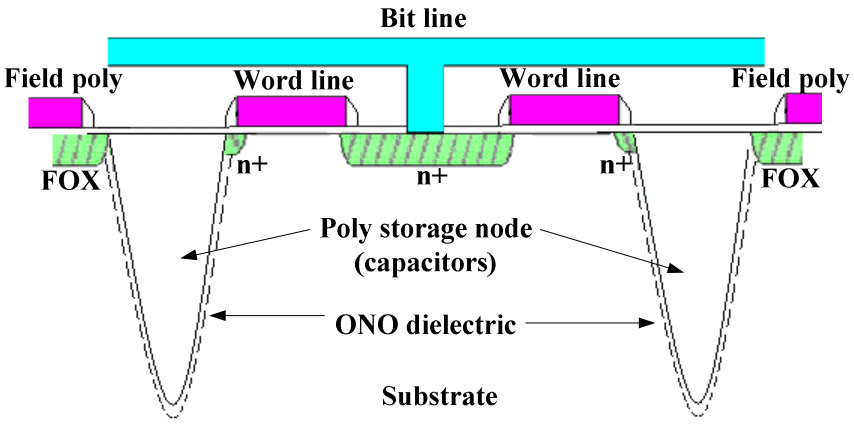


Figure 1.2 Two DRAM cells with a common bitline contact.

These limitations have led the efforts to develop chalcogenide-based NVM. The cross sectional view and schematic of a PCM cell is shown in Figure 1.2. The Phase Change Random Access Memory (PCRAM) is a resistance based technology which operates on the principle of changing the resistance of the device to define the memory state as either ‘0’ or ‘1’. The change in resistance occurs due to the change in phase of the chalcogenide material between a high resistance amorphous phase and a low resistance

crystalline phase or vice-versa. The change in phase is accomplished by heating the phase change material by passing a current through it. Since exposure to radiation does not have enough impact to heat the material to cause a change in phase, phase change memory is said to be radiation resistant. Moreover, the characteristics of a chalcogenide based PCM lend themselves to store multiple bits (multiple states) in a single cell which results in much denser memories. Further PCM can be scaled into high density arrays, has a large number of program/erase cycles, and has the potential to be more reliable than flash memory due it its resistance to radiation effects, thus making it ideal for space applications.

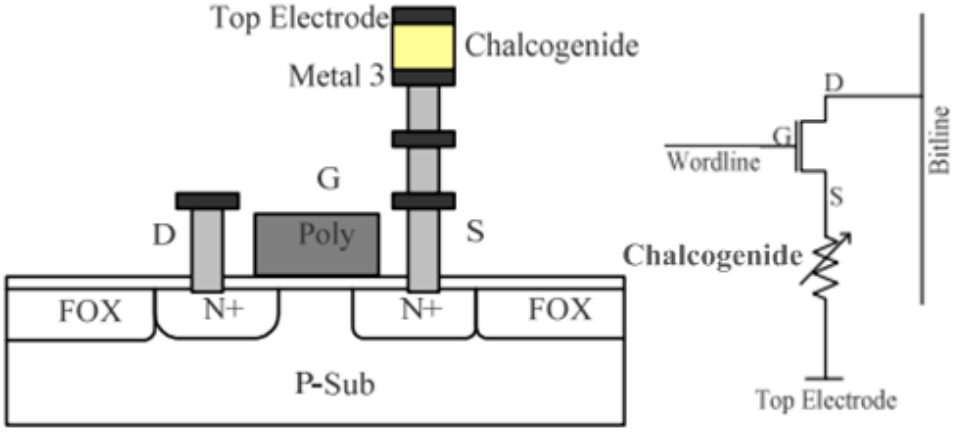


Figure 1.3 Cross sectional view of a PCM cell [2].

Memory Architecture

The memory architecture designed is for a Random Access Memory or RAM. RAM memory architecture allows any bit of data to be accessed at any time from the memory array and thus the name random access memory. The block diagram of a typical RAM is shown in Figure 1.4.

The following components make up a typical RAM architecture. A memory array with a memory cell at the intersection of a rowline (wordline) and a columnline (digit or bitline) is used to store data. Row and column logic consisting of latches, decoders and buffers are used to access the memory array and in turn access the data. To access a particular memory cell and read its data, the corresponding rowline is first selected through the row decoder and is made to go high. The buffer is used to provide the necessary drive to the line since it is periodically loaded with the capacitive memory cells. Once the rowline is selected, the column address is used to decode which columnline needs to be selected to access the required memory element. Once the column is selected, data can be read into or out of the array through the column decoder.

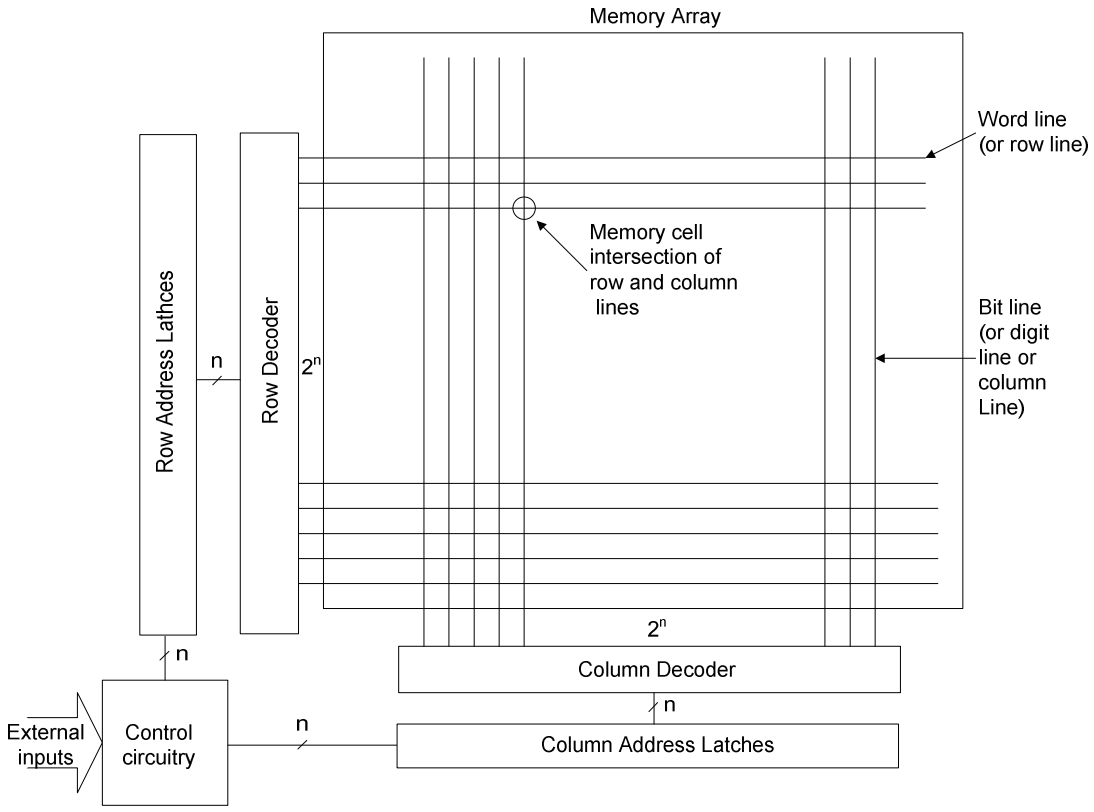


Figure 1.4 Block Diagram of RAM.

This thesis discusses circuit design and development of chalcogenide based non volatile memory and its sensing circuit. The processing methods to integrate front end-of-line (FEOL) at MOSIS [3] to backend-of-line (BEOL) at Idaho Micro Fabrication Lab (IML) [4] at Boise State are discussed.

Design of the memory architecture and its associated components are explained in detail in Chapter 2. First we focus on the design considerations of the memory elements and its access device. This is followed by a detailed discussion about the topology selected for the row and column decoders and their design. Finally the layout techniques and considerations are discussed.

Chapter 3 begins with the design of masks to be used at the Idaho Microfabrication Lab at BSU. This is followed by a brief description about the various processing steps performed at BSU.

Chapter 4 provides an introduction to Delta-sigma Modulation (DSM) based sensing techniques followed by a detailed description of the various topologies and their layout.

Chapter 5 discusses the test setup and presents the results obtained from DSM chip along with the chip micrographs. Finally, the conclusion from the research and the direction for further work is presented.

CHAPTER 2: MEMORY CIRCUIT DESIGN

The chalcogenide Memory Element – An Overview for the Circuit Designer

A chalcogenide is a chemical compound which consists of one chalcogen ion and at least one electropositive element. Chalcogens are from group 16 elements of the periodic table generally consisting of sulfides, selenides, and tellurides. The phase change memory element used in PCRAM consists of chalcogenide material sandwiched between two electrodes. As shown in the figure below, two chalcogenide layers Ge-chalcogenide (the memory layer), and Sn-chalcogenide (the metal-chalcogenide layer) are thermally evaporated over a tungsten bottom electrode to form the memory element. A tungsten top electrode is then sputter deposited to form the memory element. The processing steps are explained in detail in Chapter 3.

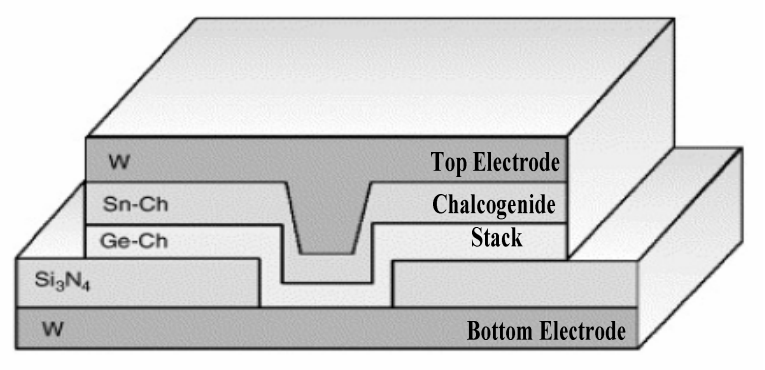


Figure 2.1 Cross sectional view of chalcogenide device structure [5].

The idea behind the use of two different chalcogenide material stacks is to reduce the voltages, currents, and switching speeds needed for phase change operation without the need for complicated physical device structure [5]. The memory element basically has two states, a high resistance amorphous state and a low resistance crystalline state. The change in state occurs due to the change in phase of the crystal orientation by Joule heating of the material through an applied current. When the phase switches from amorphous to crystalline, subsequently the resistance of the memory element changes from a high resistance to low resistance. This change in resistance is used to store data.

Theory of Operation

Most phase change materials have a threshold voltage above which the passage of current causes Joule heating which in turn causes a change in phase from amorphous to crystalline or vice-versa. This depends on several factors like the materials property, pulse duration, amplitude etc. To change the state from a high resistance amorphous state to a low resistance crystalline state, a voltage higher than the threshold voltage is applied

across the amorphous material causing the resistance to decrease significantly [6]. Due to this decrease in resistance, there is an increased current flow (SET pulse) in the device which causes Joule heating of the material. As the temperature rises above the glass transition temperature but below the melting point temperature, the current is removed, allowing the material to cool at a rate that will allow nucleation and crystal growth, transforming the amorphous volume into poly crystalline phase. The relationship beween temperature and time for the current pulses in shown in Figure 2.2.

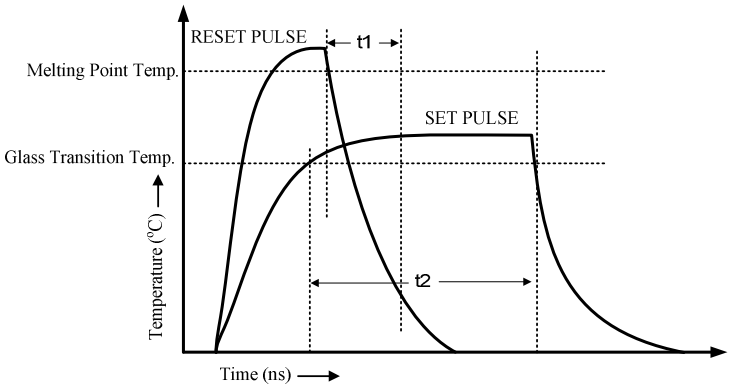


Figure 2.2 Electrical programming of a PCM [1].

The reverse transition is achieved by applying a current pulse (RESET pulse) for a shorter duration with a higher magnitude to the crystalline chalcogenide material. Once the device temperature crosses the melting point temperature, the current is quickly removed with a few nanosecond trailing edge (t1) of the current pulse as shown in Figure 2.2. Since the molten material has no time to crystallize, it is left into an amorphous state [4].

Some phase change materials have the potential to exhibit multi-state capabilities. An IV curve representation of a PCM element illustrating possible multi state operation is seen in Figure 2.3. This curve would be obtained by forcing current through the devices

and measuring the corresponding voltage across the device with a positive potential on the top electrode. The snap back regions, i.e the negative resistance, in the IV curve are characteristic of a phase change memory device [2]. Each snap back region can be associated with a memory state and thus multi state capability. For each snap back region, the resistance increases to a certain maximum value, and a further increase in current cause an abrupt reduction in the resistance causing the voltage to decrease drastically.

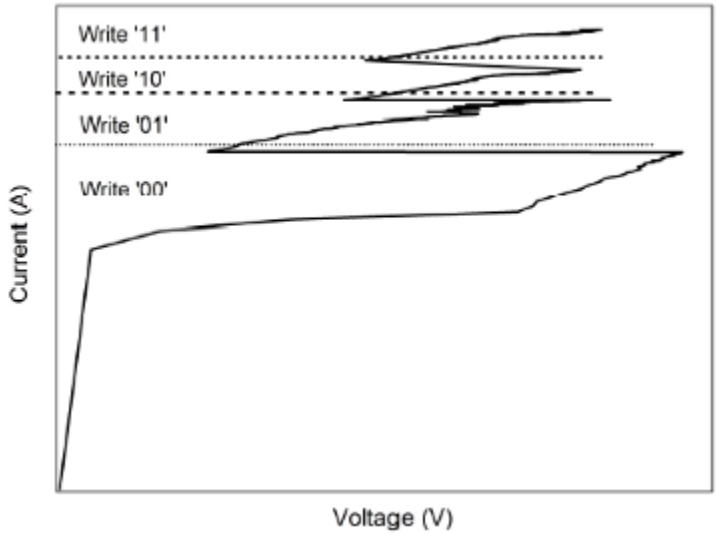


Figure 2.3 IV curve representation of a PCM bit with possible multi state capability [2].

Figure 2.4 shows an example non-overlapping resistance distribution in a PCM cell. The figure shows four stable resistance states which can be used to store two bits of data. The number of stable resistance state determine the number of data we can store in a single cell [2]. This depends on the number of crystalline/amorphous phases available in the chalcogenide material.

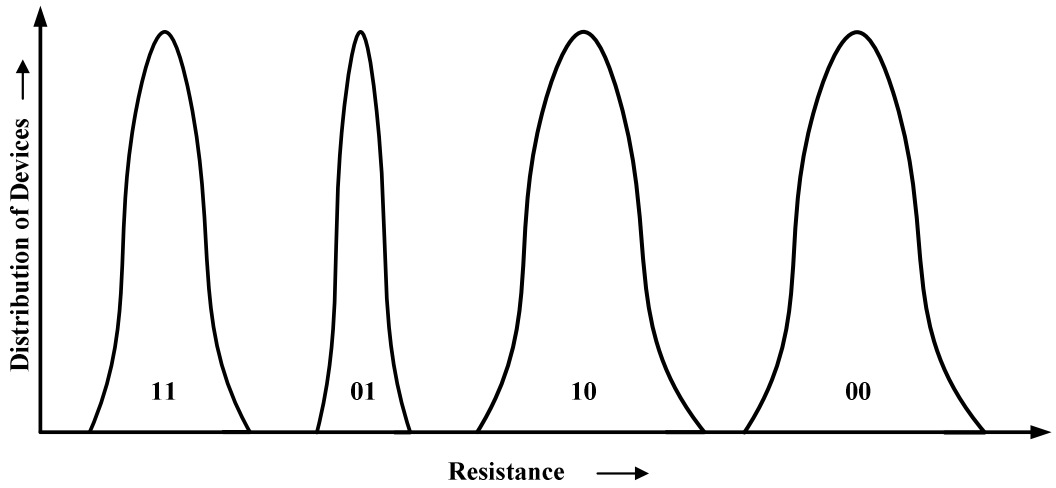


Figure 2.4 An example distribution of states based on resistance [2].

Memory Bit and Access Transistor

The memory bit consists of an NMOS device as the access transistor and a chalcogenide memory element. The NMOS acts as an isolation device when laid out in an array. An NMOS device was preferred over a PMOS device because of its larger drive current which is an essential requirement for exhibiting multi state capabilities. Figure 2.5 shows the schematic and its corresponding layout view for a single memory bit. The gate of the MOSFET is used for the wordline and the drain terminal is connected to the bitline when used in a memory array. The PCM element is connected to the source terminal and the other end is connected to a top electrode which would be common to all the memory bits in the array. For programming the cell the gate (Wordline) voltage is set high and a current pulse is passed through the drain (bitline) of the access MOSFET which heats the chalcogenide on the source side causing a change in state and eventually storing data.

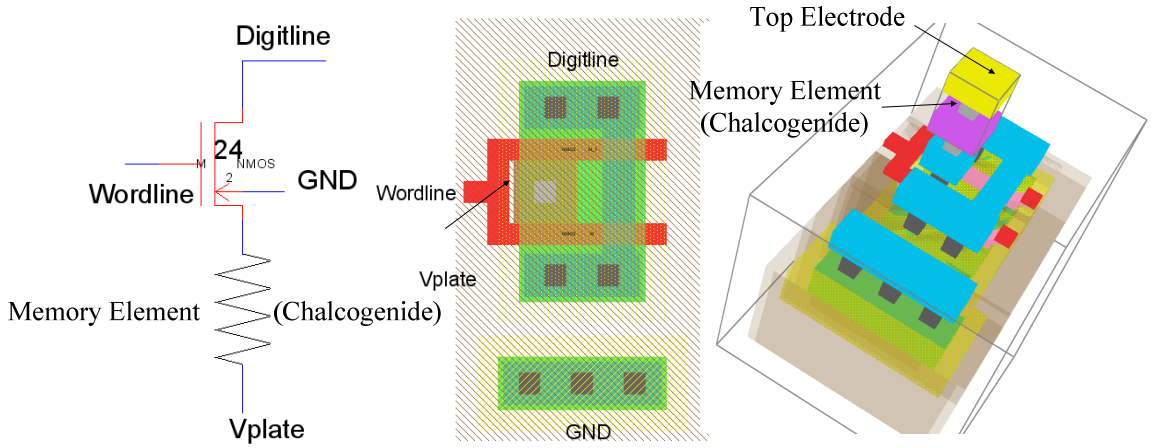


Figure 2.5 Schematic and layout of memory bit.

Design and Layout Considerations

The layout of the memory devices and circuits were done in AMI C5 process through the MOSIS fabrication service. To ensure adequate drain current a NMOS device size of 32/2 was selected. With the scale factor being 300 nm, the actual size of the device comes up to 9.6 µm by 0.6 µm. The I_D vs V_{DS} simulation results from Figure 2.6 show a maximum drive current of 4 mA for the NMOS of 32/2.

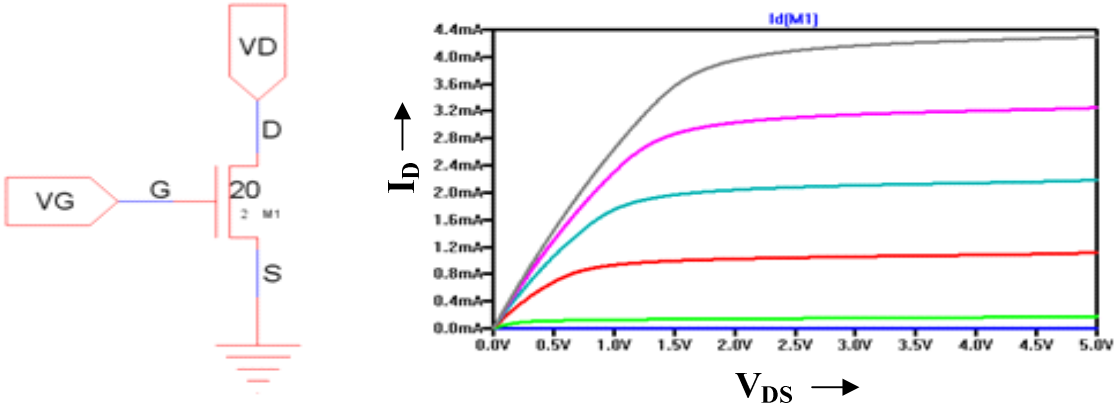


Figure 2.6 IV characteristics of a 32/2 NMOS.

The fabrication of the memory device was envisaged to be performed using two separate processing services. The front end-of-line (FEOL) consisting of the fabrication of the MOSFET and major interconnects are performed through the MOSIS service. The backend-of-line (BEOL) consists of the deposition and pattering of the chalcogenide and the top electrode was performed at the Idaho Micro Fabrication Lab at Boise State University. This is explained in detail in Chapter 3.

The cross sectional view of the memory bit used in the test structure is shown in Figure 2.7. Since the AMI C5 process is a three metal process, the MOSIS service is used to fabricate the device until Metal 3. The PCM bit placed on top of Metal 3 (bottom electrode) and a tungsten metal plate on top of the PCM bit (top electrode) are fabricated at the Idaho Micro Fabrication Lab. Since the chalcogenide is deposited on top of Metal 3, the size of the PCM bit depends on the size of the Metal 3 bottom electrode in the layout submitted to MOSIS.

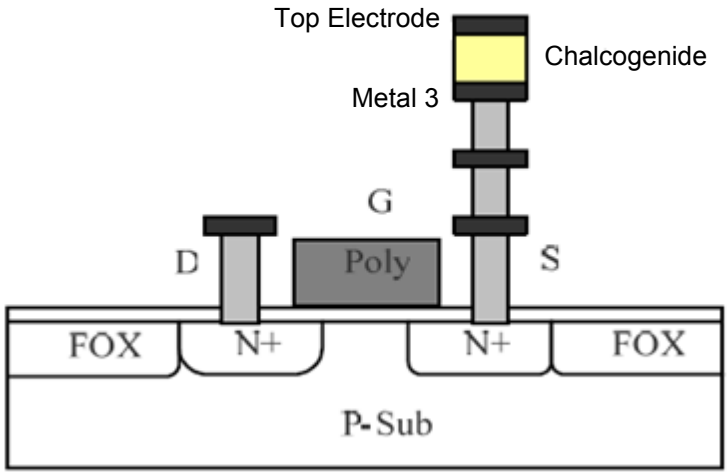


Figure 2.7 Cross sectional view of memory bit showing chalcogenide [2].

The design and layout of the memory bits were done using Electric VLSI Design System [7]. The 32/2 NMOS was laid out using two fingered MOSFETs with drawn

widths of 16 each. The size of the memory bit layout is 1.2 μm square. The layout submitted to MOSIS for the BEOL processing consists of the above said MOSFET with metal interconnects up to Metal 3 for all the four terminals (Gate, Drain, Source and Body). The Gate, Drain and Body were connected to bond pads on Metal 3 with passivation on top for external bonding. The source connection was terminated on Metal 3 with passivation on top for chalcogenide deposition.

Figure 2.8 shows the layout of a single memory bit with its corresponding terminals. A bond pad size of 75 μm by 75 μm was deemed adequate to make contacts to the Gate, Drain and the Source terminals on Metal 3. The bottom electrode size for the memory bit was chosen to be 1.8 μm by 1.8 μm and was provided on Metal 3 on the source terminal. A passivation opening of 42 μm by 42 μm was provided on top of the bottom electrode for the deposition of chalcogenide.

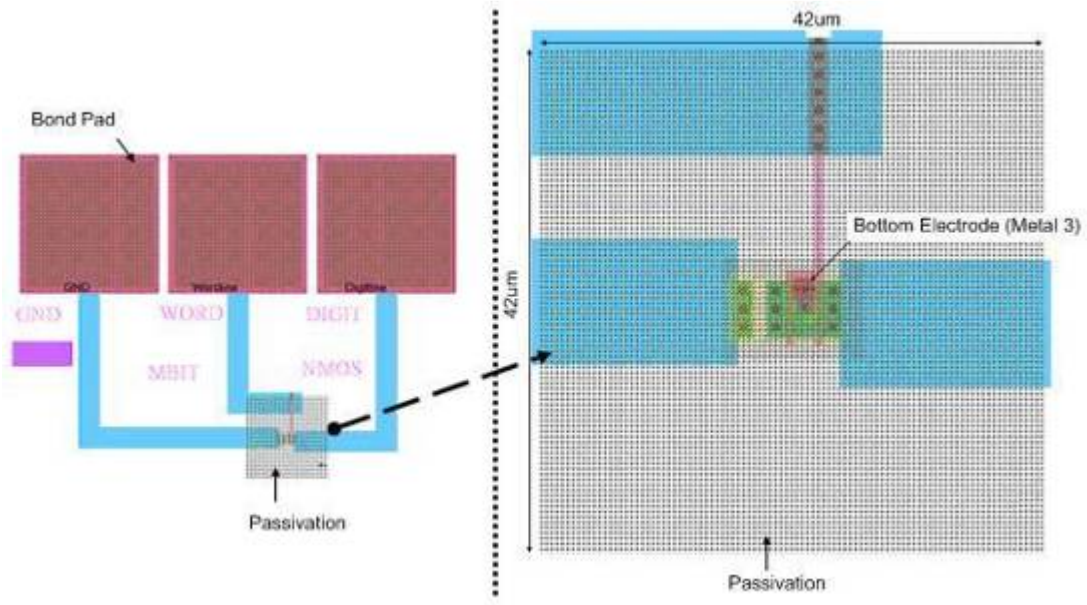


Figure 2.8 Memory bit layout.

Memory Array Design and Layout

Typical memory architecture consists of memory array along with its peripheral circuitry. The memory array fabricated for reliability investigation of chalcogenide based PCRAM consists of an 8×8 matrix of memory bit forming a basic 64 bit memory array. A 1T-1R cell topology was adopted for the memory array. The memory bits used in the array shown in Figure 2.9 consists of 32/2 NMOS isolation device with 1.8 μm by 1.8 μm bottom electrode size for the PCM bit, thus the cell topology 1T-1R. The peripheral circuitry consisting of the row and column decoders are explained in the next section. Sensing is done off chip and is explained in detail in Chapter 4.

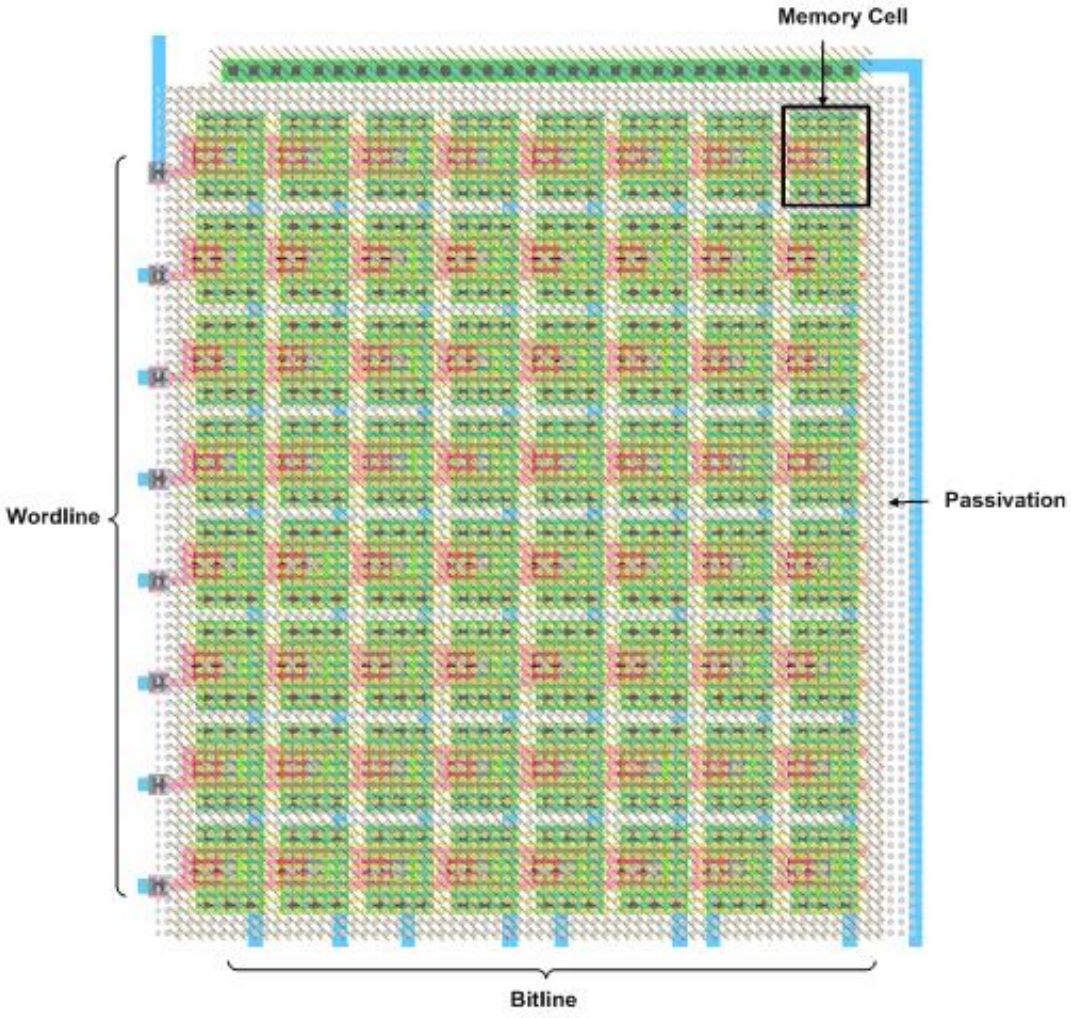
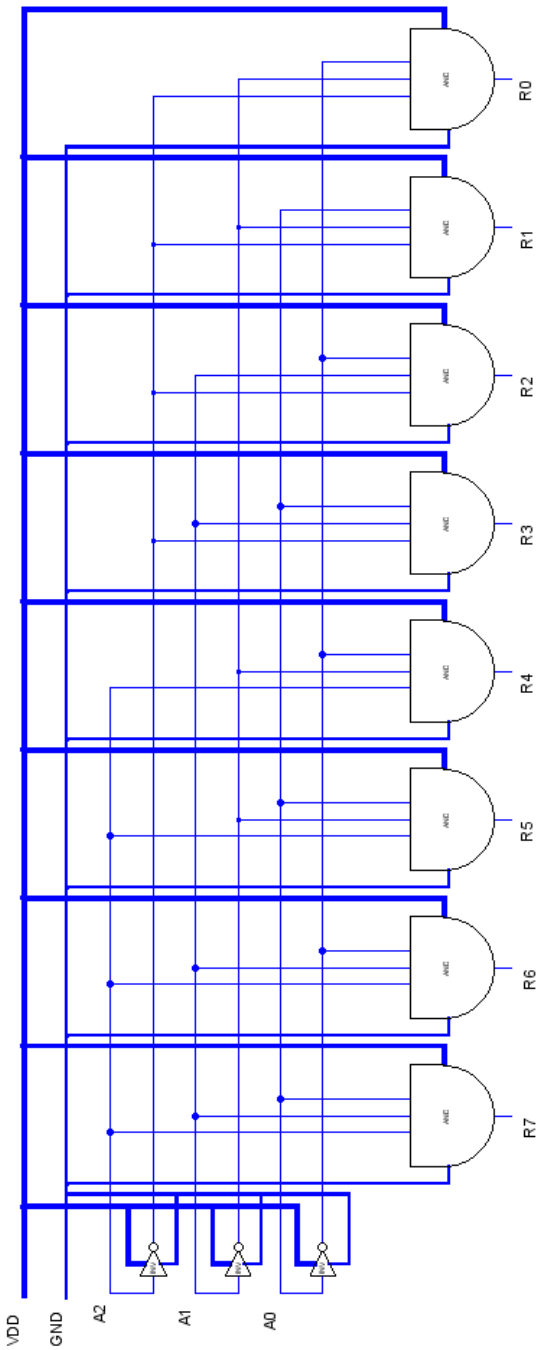


Figure 2.9 Memory array layout.

Row and Column Decoder

A static decoder topology as shown in Figure 2.10 was used for row decoder circuit. The n-to-2^n type binary decoder uses combinational circuits to convert binary information from 'n' coded inputs to a maximum of 2^n unique outputs. To drive the 8 rowlines/wordlines (R0-R7) of the 64 bit array, a 3-to-8 decoder is employed. The associated truth table and simulation results are shown in Figure 2.10 and 2.11.



Selected Wordline	A2	A1	A0
R0	0	0	0
R1	0	0	5V
R2	0	5V	0
R3	0	5V	5V
R4	5V	0	0
R5	5V	0	5V
R6	5V	5V	0
R7	5V	5V	5V

Figure 2.10 Row decoder schematic.

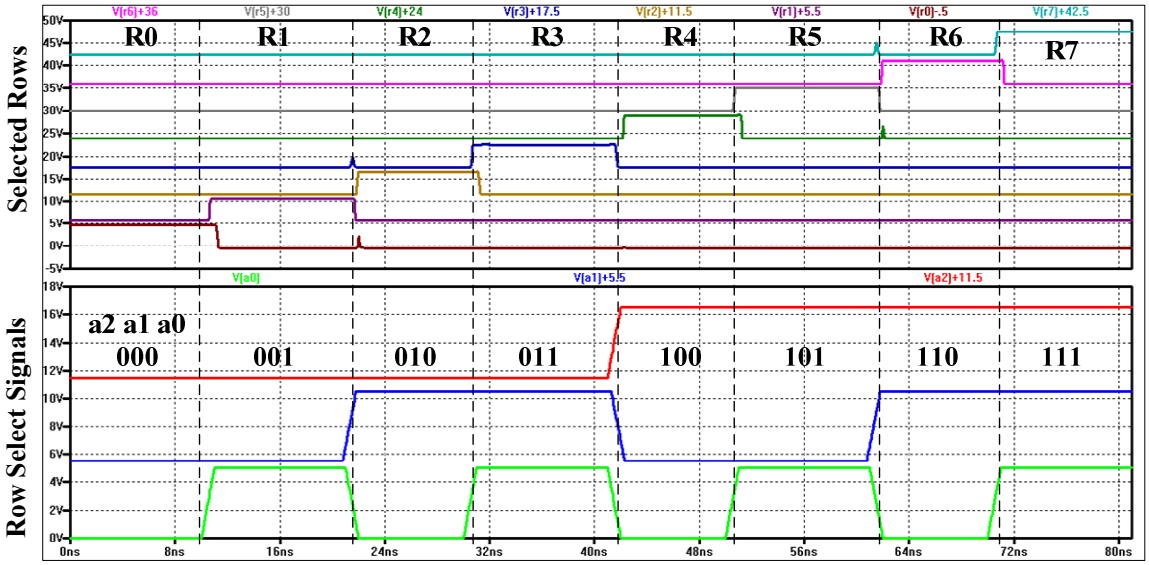
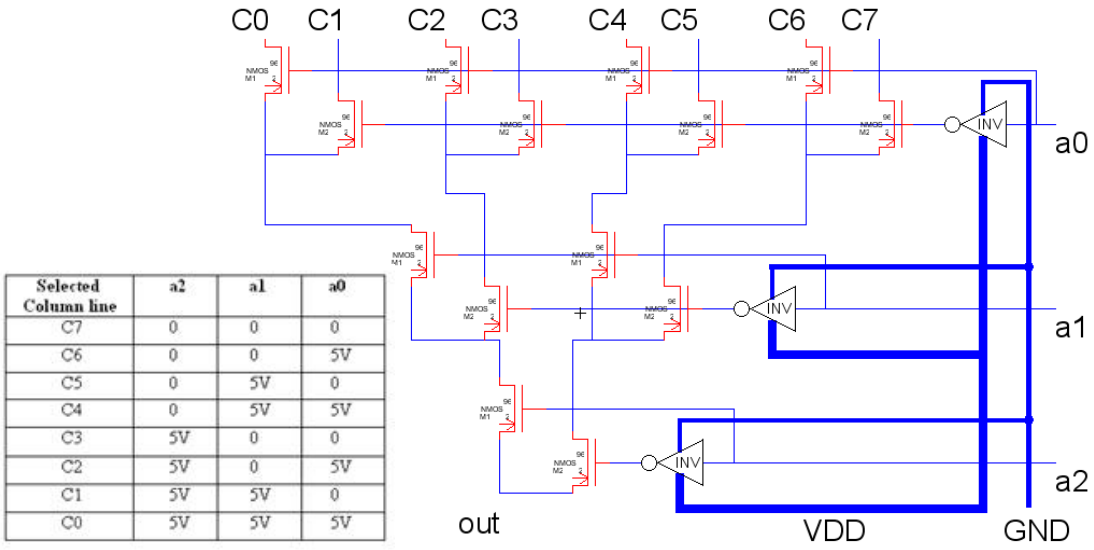


Figure 2.11 Row decoder simulations.

For the column decoder, a pass-transistor based tree decoder is used. Since the column decoder must be able to read or write data to the memory cells, pass transistors are used. The drawback in using this topology is the NMOS pass-transistor does not pass a logic one to a full logic level. This limitation though does not effect the memory operation since, during program/erase cycles, the column decoders are used to pull the drain of the desired memory cell to ‘gnd’ and other memory cells to about 3 V to inhibit them from getting programmed/erased. In either case the threshold drop of the NMOS pass-transistor does not effect regular operation. The column select signals a0-a2 in Figure 2.12 connects the desired bitline to the decoder output during the sense operation and to ground during program/erase cycles. Figure 2.13 shows the simulation result for the column decoder.



Selected Column line	a2	a1	a0
C7	0	0	0
C6	0	0	5V
C5	0	5V	0
C4	0	5V	5V
C3	5V	0	0
C2	5V	0	5V
C1	5V	5V	0
C0	5V	5V	5V

Figure 2.12 Column decoder schematic.

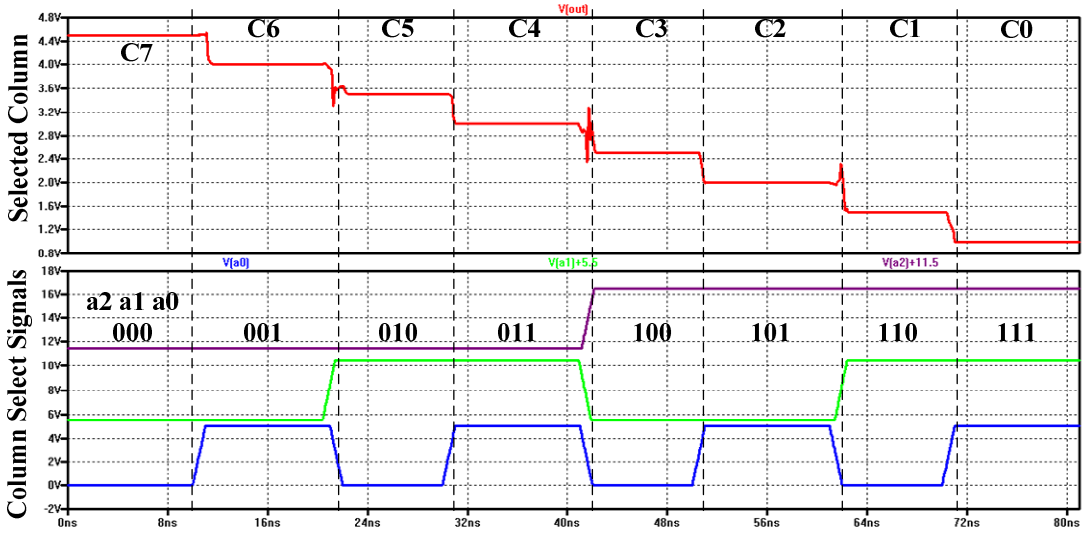


Figure 2.13 Column decoder simulations.

Figure 2.14 shows the layout of the complete memory array along with its peripheral circuitry that includes the row and column decoder. This figure is analogous to the block diagram of the RAM architecture presented in Figure 1.1 of chapter 1. The row and column decoder were designed to show proof of concept of the memory array

operation for PCRAM. Hence much effort was not put into making the design or the layout any compact. Note that the chalcogenide and Tungsten top electrode will be blanket deposited over the entire array during BEOL.

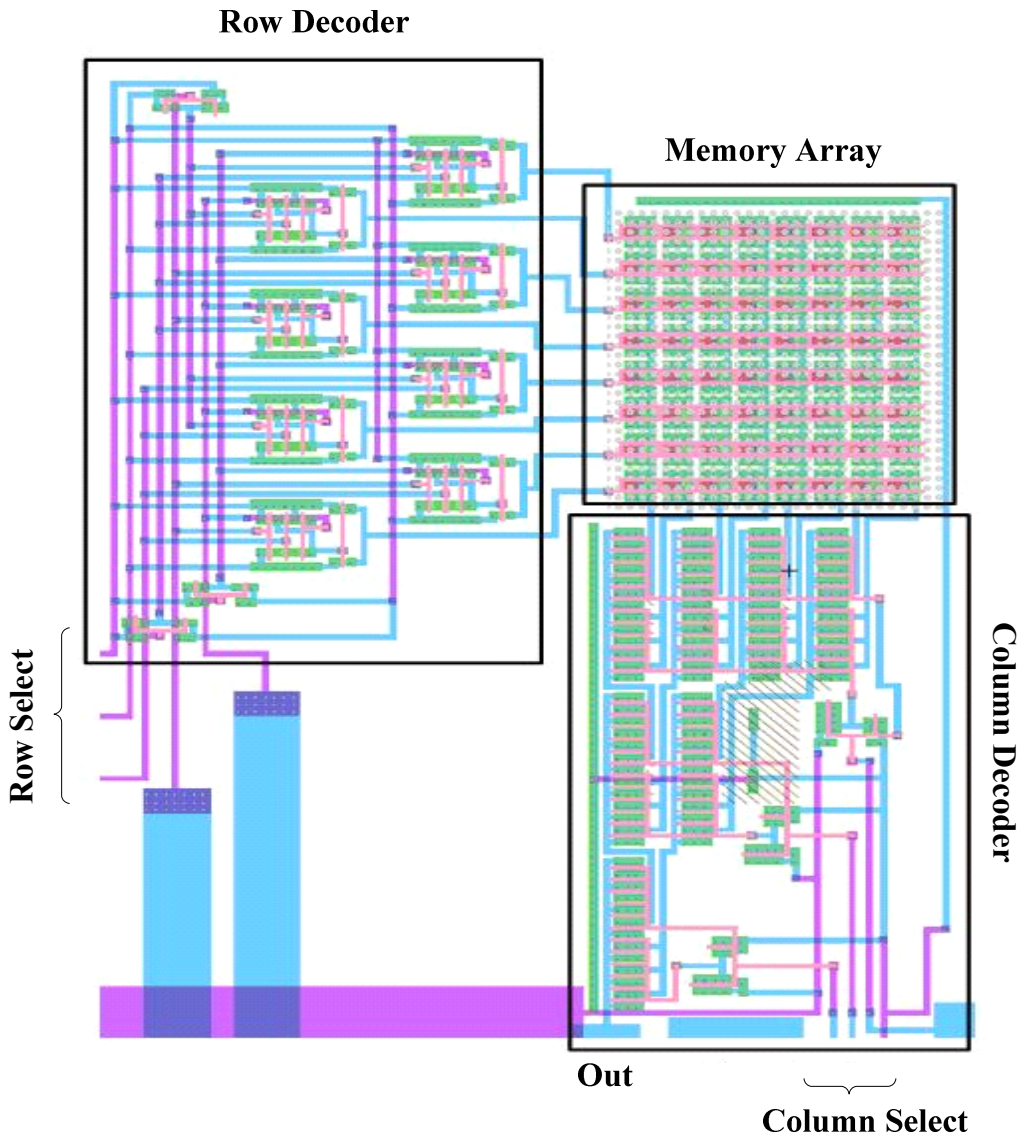


Figure 2.14 Memory array and peripheral circuitry layout.

For programming or erasing a memory cell, the row select signal makes one of the wordlines high. Similarly the column select signal connects one of the bitline to ground. A voltage higher than the threshold voltage is applied to the top electrode causing current to flow through the desired memory cell thus switching the memory cell to programmed or erased state. Similarly, during the sense operation the desired wordline is driven high using row select signals and the bitline is connected to the sense-amplifier by the column select signal. A voltage much lesser than the threshold voltage is applied to the top electrode causing a small current to flow through the memory cell. The current is small enough not to change its state. This current is used to sense the state of the memory cell and is explained in Chapter 4.

Summary

Chalcogenide based phase change memory works on the principle of Joule heating and has the advantage of being resistant to radiation effects. It also has the capability of storing multiple bits on a single memory cell depending on the number of stable, non-overlapping resistance states available in chalcogenide device. Various design considerations were taken into account for integrating two discrete processing services for the fabrication of the PCRAM cells. Several test structures including a 64 bit memory array, single memory bits of various bottom electrode sizes and access transistors with and without the memory bits were included in the layout to study and characterize the access devices, memory bits and the performance of the array.

CHAPTER 3: MASK DESIGN AND BACK END OF LINE PROCESSING

The chips obtained from MOSIS were subjected to a series of post processing steps at Idaho Microfabrication Lab at Boise State University. The integration of the MOSIS fabricated chip with the post processing procedures at IML is explained in this chapter.

Figure 3.1 shows the picture of a bare die obtained from MOSIS showing the passivation opening for chalcogenide deposition. The test chip consists of a memory array, two terminal memory devices (Mbits) also called resistor bits and memory element with access transistor to study and characterize PCRAM. The chip also consists of transistors for characterizing the effect of BEOL processing on their operation.

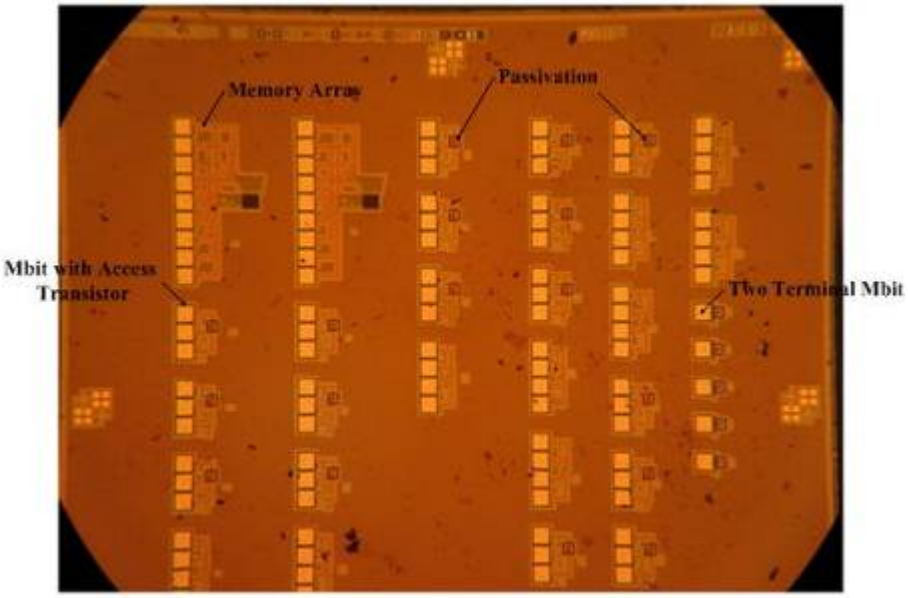


Figure 3.1 Bare die obtained from MOSIS.

Mask Design

The mask design for the BEOL processing was performed using Electric VLSI Design System. It was then sent for fabrication to Rochester Institute of Technology Semiconductor & Microsystem Fabrication Laboratory Mask House [8]. A clear field mask tone [9] was used in the mask design for patterning the chalcogenide and top electrode. Hence the feature (chalcogenide/top electrode) in the mask is defined as being chrome and the field as clear.

Design Criteria

Figure 3.2 shows the layout of the chip and the mask for pattering the chalcogenide and top electrode. In the figure of the mask on right, all the features seen are made in chrome and hence the mask is said to be a clear field mask. There were several processing concerns taken into account prior to the mask design. To start with, the mask design should be in accordance with the equipment available at IML at Boise State University. The resolution limitation of the Quintal Q-4000 contact aligner required the mask design to have a 20 μm tolerance. This meant a misalignment of even 20 μm would still result in proper contact of the bottom electrode with chalcogenide. This is illustrated in Figure 3.3 and 3.4. A positive photoresist was selected for patterning the chalcogenide and top electrode. Since the part of the photoresist exposed to light would be removed by using a positive photoresist, a clear field mask with chrome feature representing the top electrode was chosen for the mask design. Also, layout text were incorporated in the

mask for providing site number and other details of the test structures as illustrated in Figure 3.3 and 3.4.

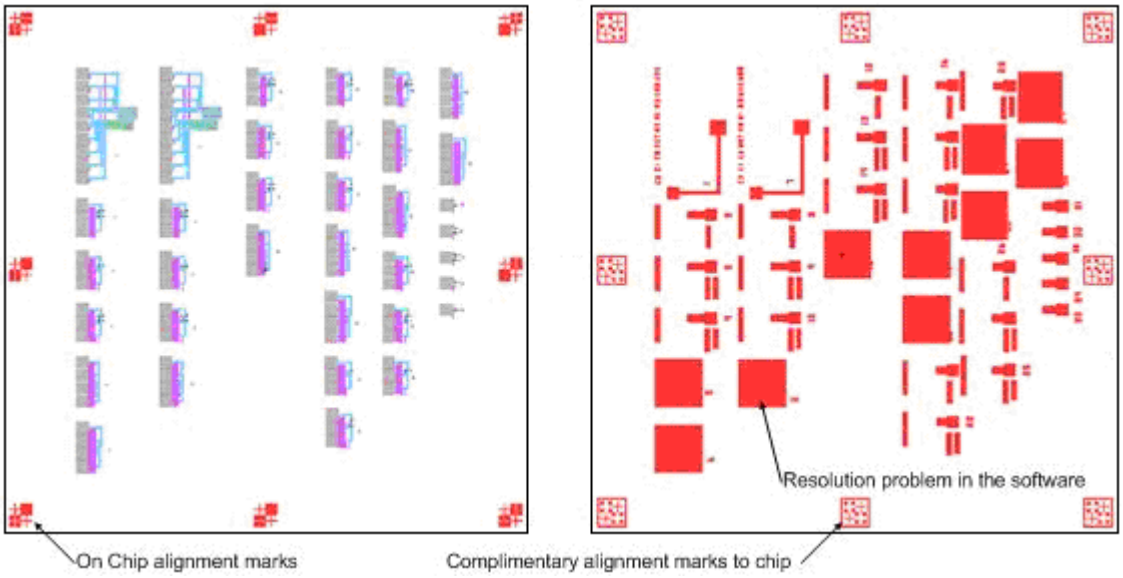


Figure 3.2 Layout view of chip and mask from Electric VLSI Design System.

Figure 3.3 shows the alignment of the mask for patterning chalcogenide and top electrode on the Mbit test structure while illustrating the 20 μm tolerance. Layout texts are also seen on the figure, which were included in the mask to give details about the particular test structure. It was ensured during the design that a misalignment does not cause the layout text to overlap adjacent test structures.

Figure 3.4 depicts a properly aligned and a misaligned mask with a test structure. Even though the figure on the right is misaligned we see that adequate contact is still ensured between the bottom electrode and chalcogenide/top electrode and hence the reason for providing the 20 μm tolerance. The via shown in Figure 3.4 is the bottom electrode with the passivation on top forming a via like structure where the chalcogenide is deposited. Also seen in the figure are the layout texts as seen from the microscope.

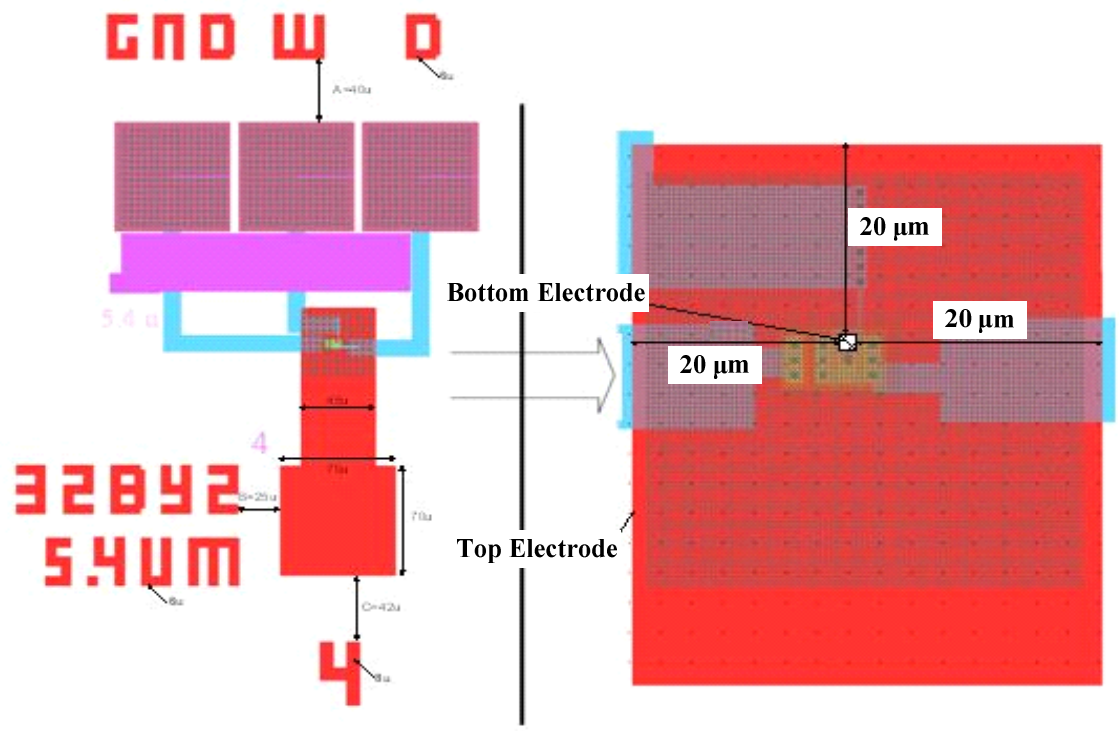


Figure 3.3 Layout image of an Mbit test structure showing the 20 µm tolerance of top electrode mask and the associated layout text.

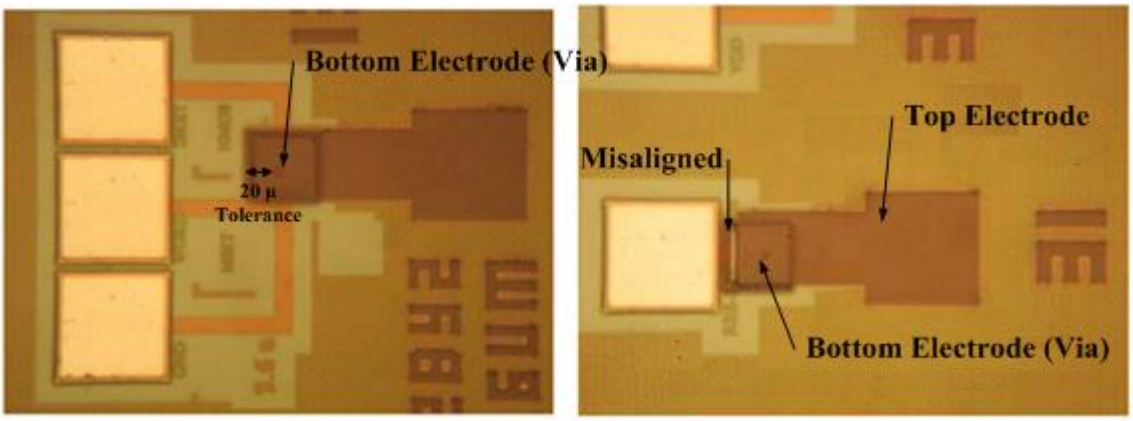


Figure 3.4 Chip images of an aligned and a misaligned top electrode with bottom electrode.

Figure 3.5 shows the aligned image of mask with the die both in design/layout view and original image seen through a microscope after post processing.

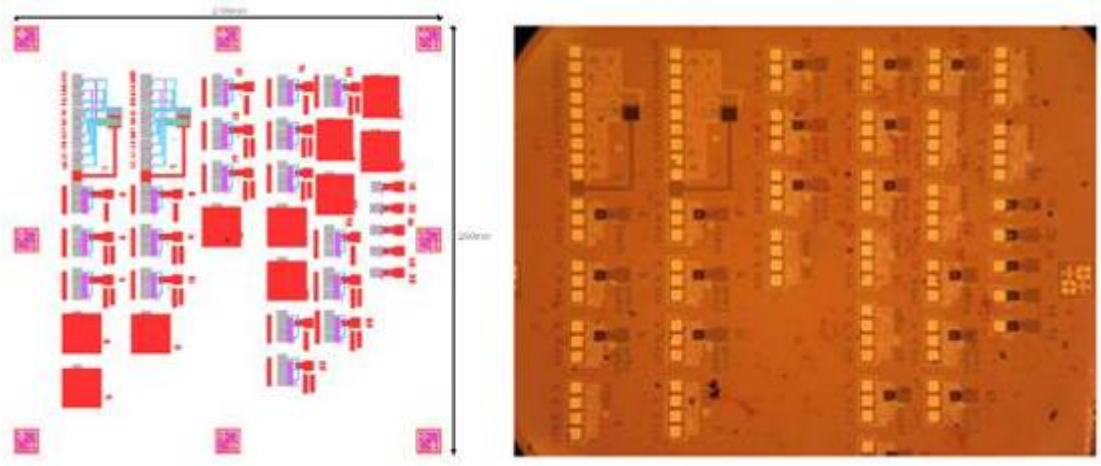


Figure 3.5 Mask and die aligned in layout/design view and from a processed die.

The alignment marks on the mask are made complementary to those in the chip to align the mask and the die. Figure 3.6 shows alignment marks from the mask and chip aligned together. The alignment marks were designed with smaller error margins of 10 μm which is much lesser than the device tolerance of 20 μm. This ensures adequate coverage of chalcogenide and top electrode over device vias.

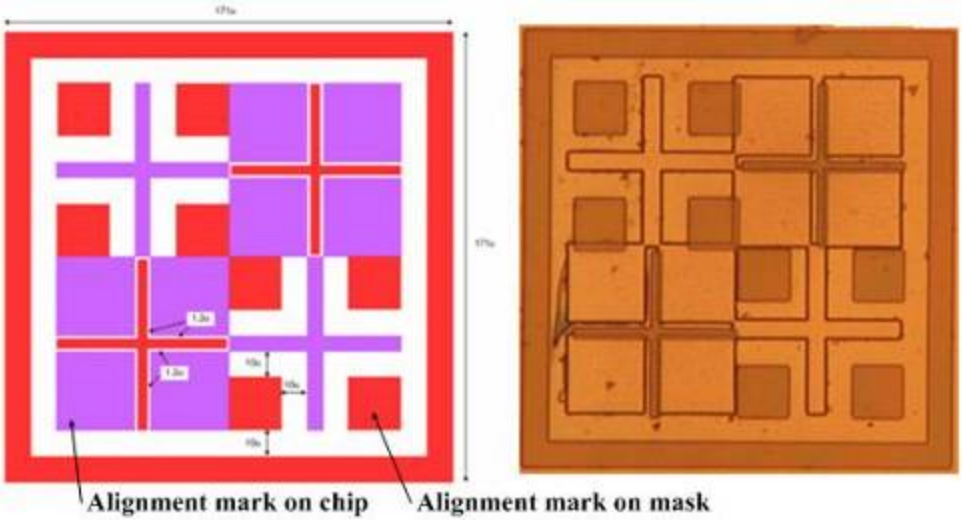


Figure 3.6 Alignment marks on chip and die aligned in layout view and chip image.

A 12 to 18 μm tolerance is shown in Figure 3.7 describing the mask design for the test structure containing the memory array. Also seen the figure is layout text describing the test structure and bond pad details.

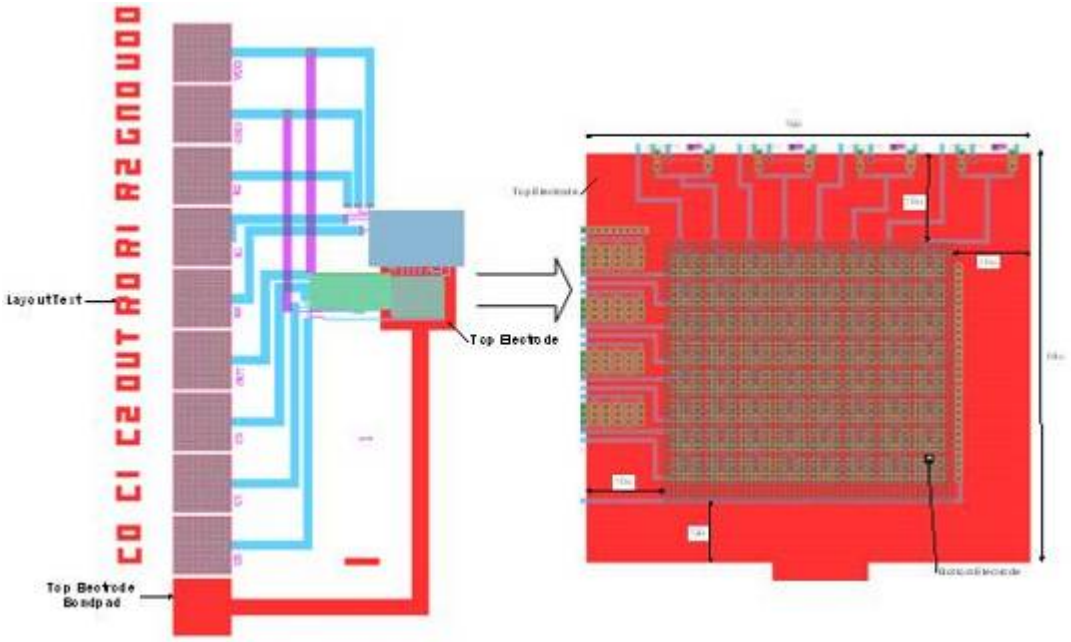


Figure 3.7 Mask and die aligned in layout/design view.

Back-End-of-Line Processing

The Back-End-of-Line processing steps were performed at Idaho Microfabrication Lab by Jennifer K. Regner, Beth Cook, Yingting Li, Hiwot Kassayebetre and Anshika Sharma of Electrical and Computer Engineering department under the guidance of Dr. Kristy A. Campbell and Dr. R. Jacob Baker. Upon receipt of the die from MOSIS, the chips were visually inspected and electrical data was collected from the transistors specifically laid out in the die for characterization. I_D-V_{DS} tests were performed and recorded to study the I_D variation in the transistor which is one of the main concerns in the operation of a memory bit. This measurement also gives a base value to compare the effect of post processing steps on the transistors.

Prior to the processing steps on the die, the die is fixed to a 100 mm wafer using Ablebond epoxy 84-3 and is cured in a muffle furnace for 150 ºC for an hour to ensure proper bonding of the die to the wafer. The epoxy bonding of the die to the wafer enables easy alignment of the mask to the die using the alignment marks on the die and mask. It also makes it easier to handle the die while performing the various processing steps.

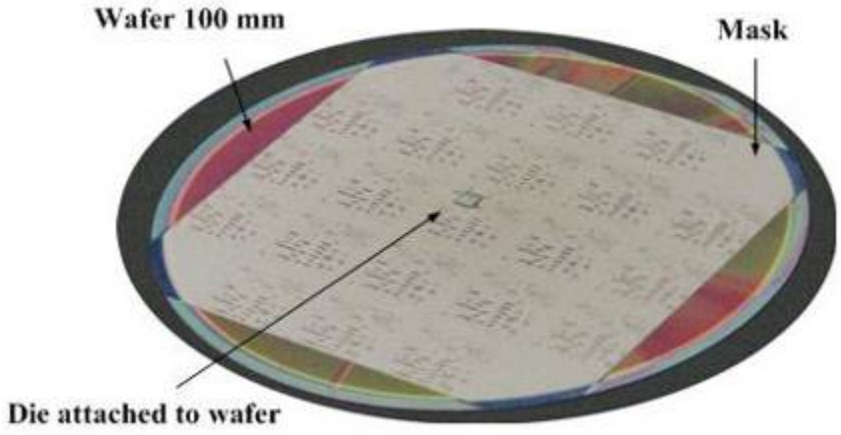


Figure 3.8 Single die attached to a 100mm wafer.

Post Processing Steps

Figure 3.9 describes the general process flow of the BEOL processing performed at Idaho Microfabircation Lab. Note that the bare die is sputter cleaned using Ar^+

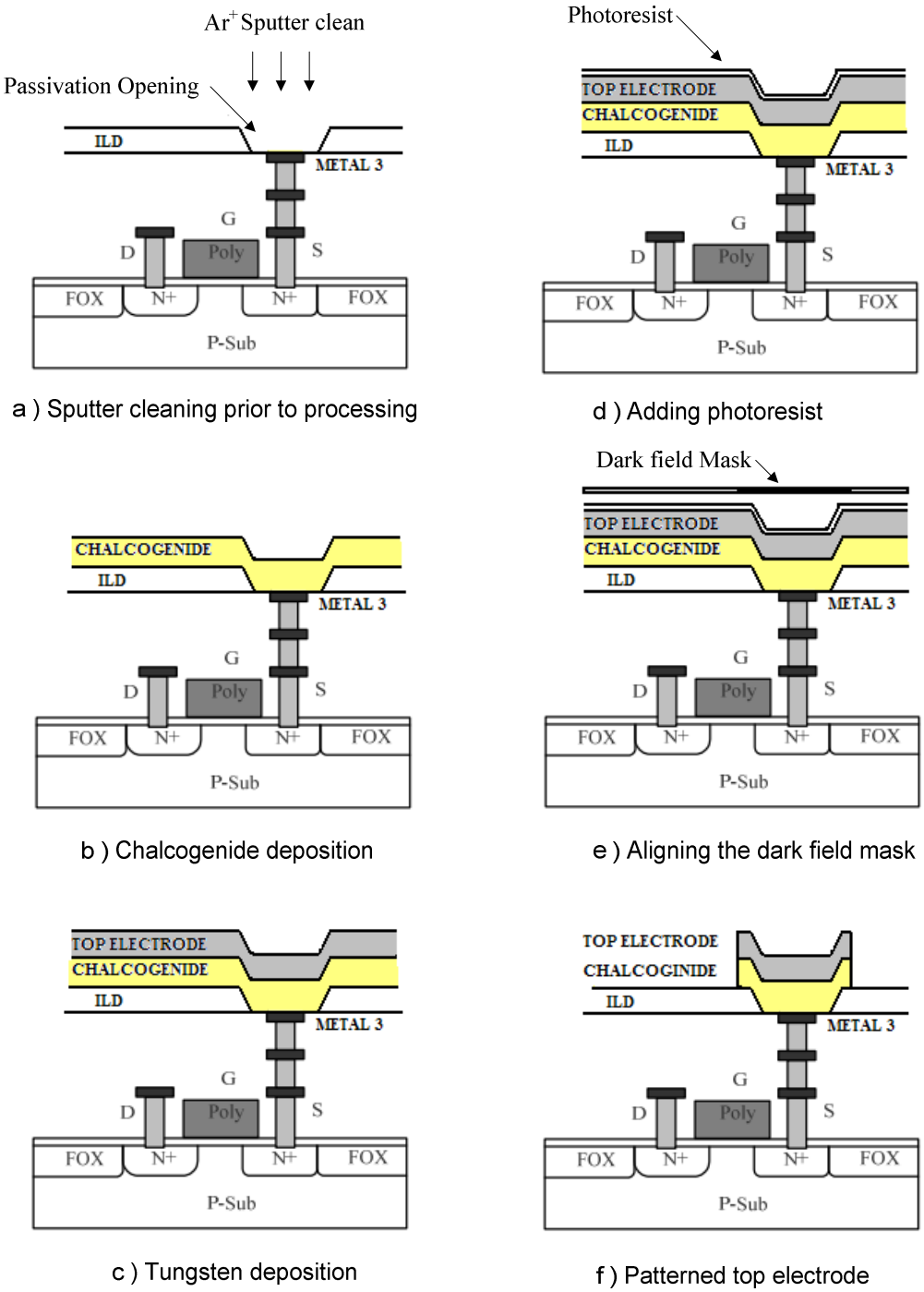


Figure 3.9 Sequence for BEOL processing of the die.

The die is first sputter cleaned with Ar^+ to remove any metal oxides from the exposed Metal 3 due to the passivation opening. The sputtering operation is performed using a Veeco ME 1001 ion mill with 550 eV beam voltage, 300 eV source voltage, 300 mA beam current and -45^o etch angle, with a process time of 6 s [10]. After sputter clean, chalcogenide films are thermally evaporated within 24 hrs. The evaporation process is done using a CHA industries SE-600-RAP evaporator with three-wafer planetary rotation at a base system pressure of 2×10^{-6} Torr [10]. The deposition rate is monitored with a single crystal head Inficon IC 6000. The dies are processed with different stacks of chalcogenide as described by Campbell and Anderson [11]. The memory stack consists of 300 Å Germanium Selenide followed by 500 Å SnTe (Alfa Aesar) with an air break between films. Memory stacks consisting of SnSe instead of SnTe were also deposited and tested in the other dies. This step was followed by tungsten sputter to form the top electrode. The tungsten film was sputter deposited at 50 watts power, 8×10^{-6} Torr base pressure (350 Å), in a Sputter Sciences CrC150 single wafer tool [10].

The deposition of tungsten is followed by a photolithography process to define the top electrodes. A Quintel Q-4000 Contact Aligner is used to align the die with the mask. Figure 3.10 shows the image of the die aligned with the mask. The photolithography to define, the top electrode and bond pads are performed using Megaposit SPR-220.30 photoresist and Megaposit MF-26A developer. An Ar^+ ion mill etch is performed using a Veeco ME 1001 ion mill with 550 eV beam voltage, 300 eV source voltage, 300 mA beam current and -45^o etch angle, with a process time of 6 s [10]. This etch defines the top electrode for the memory bits. Figure 3.11 shows a fully processed die with visible top electrodes.

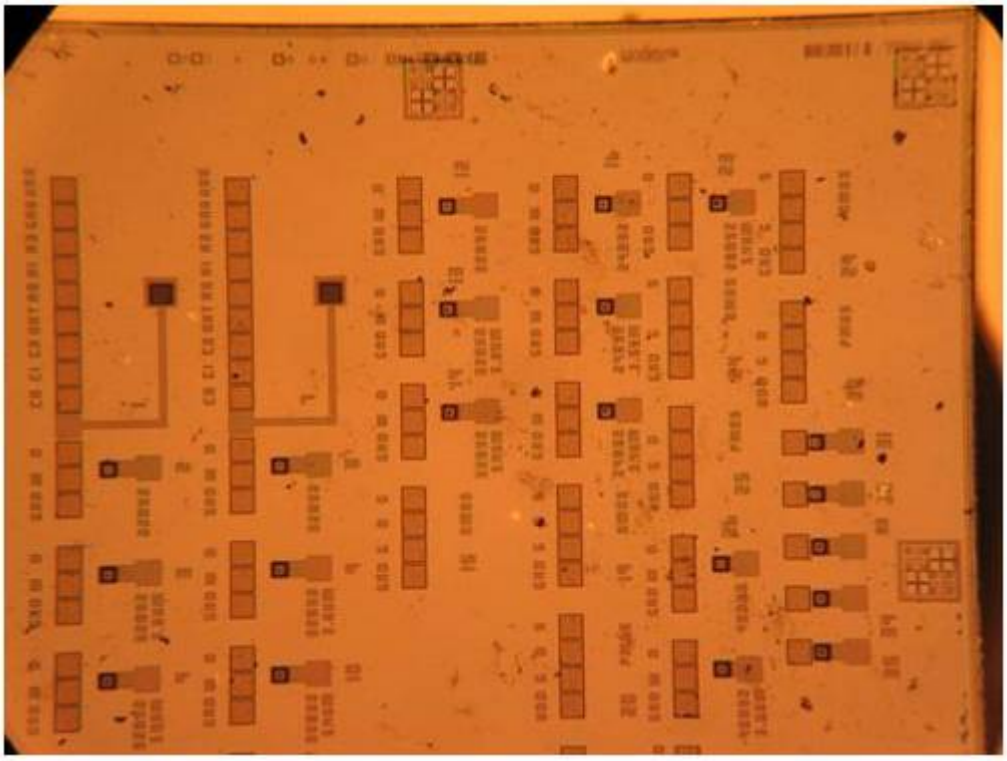


Figure 3.10 Image of the die aligned with the mask.

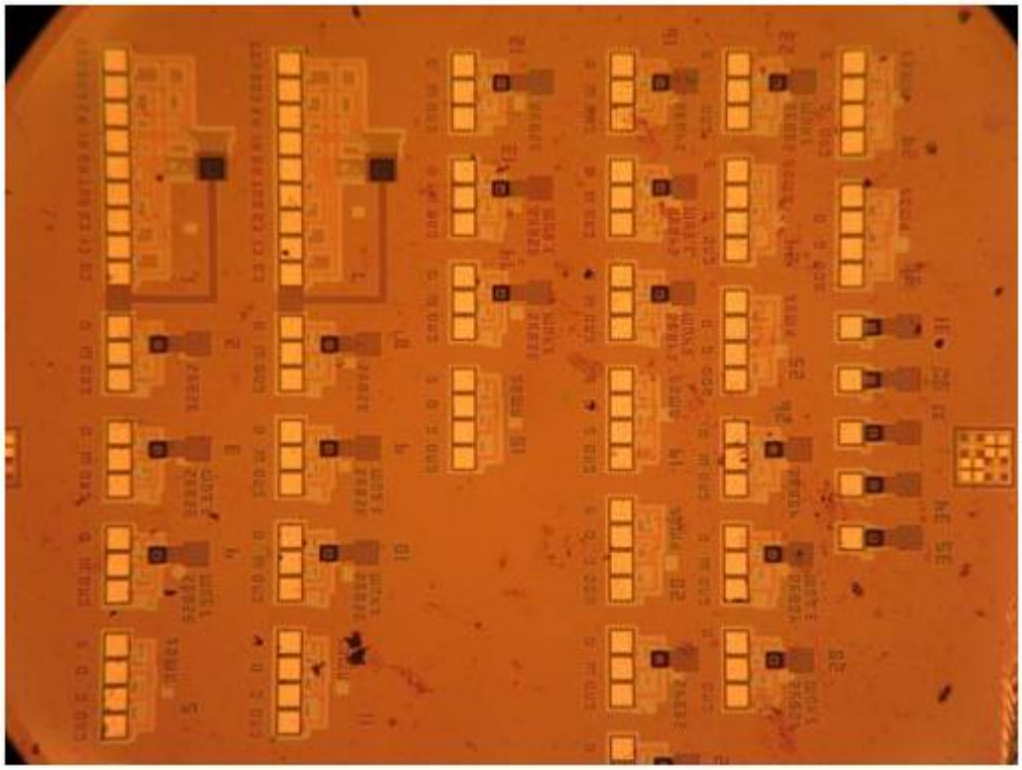


Figure 3.11 A processed die with visible top electrode.

Electrical Characterization

The processed die were subjected to electrical characterization prior to the BEOL processing and after the processing steps. Characterizing the transistor prior to the BEOL processing helps determine the effects of the processing steps on its operation. Figure 3.12 shows the IV curve of a 28/2 NMOS access transistor from design simulation. This simulation results are compared with the IV curves obtained from the die, pre and post BEOL processing in Figure 3.13. The electrical characterization was performed using an HP4145B semiconductor parameter analyzer. Comparing Figures 3.12 and 3.13, we see that there is not any significant effect on the electrical characteristics of the transistor from the processing steps. We also see that the model used for the simulation in Figure 3.12 during the design phase matches pretty closely with the actual IV curves obtained from the die.

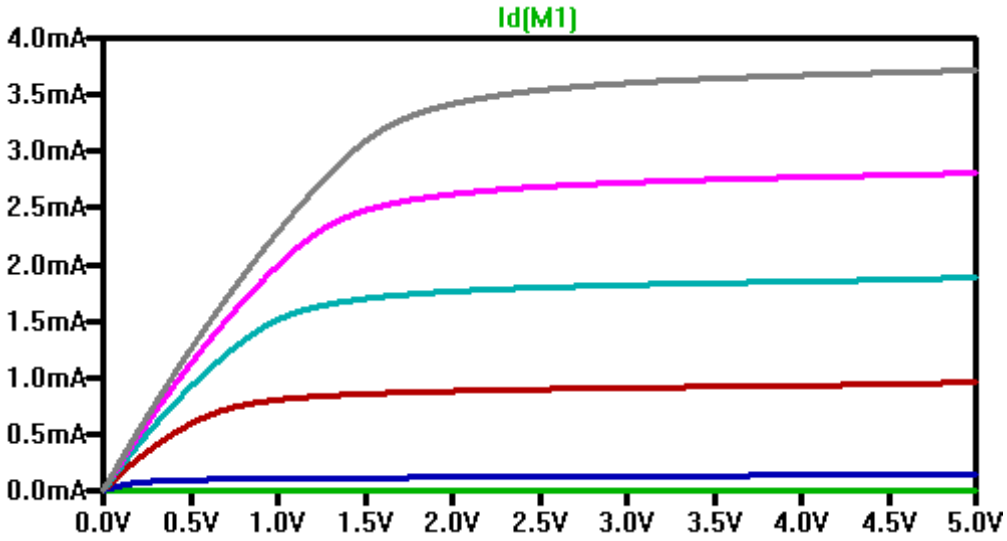


Figure 3.12 IV curves of NMOS access transistor from design simulation.

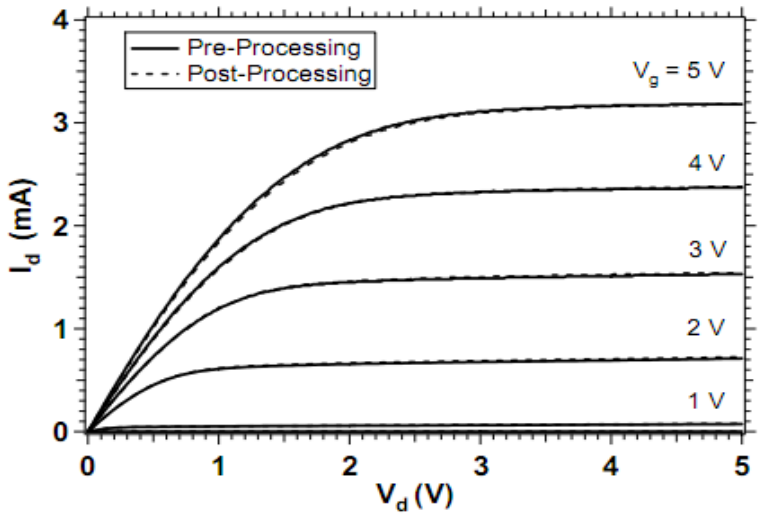


Figure 3.13 IV curves for 28/2 NMOS access transistor pre and post BEOL processing [10].

To characterize the phase change material, a current was forced though a two terminal device consisting of a stack of Ge_2Se_3/SnSe and the voltage drop across the chalcogenide stack was measured. Figure 3.14 shows the IV curve for two terminal memory stack described above. The via size for the memory stack tested was 1.8 μm by 1.8 μm.

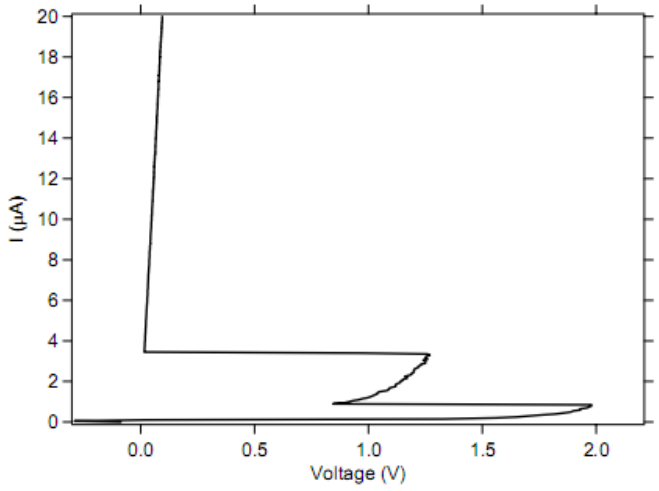


Figure 3.14 IV curve from Ge_2Se_3/SnSe two terminal devices [10].

Figure 3.14 illustrates the possible multi state operation of the memory stack evident from the two snap-back regions. This is similar to the multi state operation described in Chapter 2 in Figure 2.3.

Sensing techniques for this resistive memory are discussed in the next chapter.

Summary

Commercially available CMOS processes can be successfully integrated with in-house post processing techniques for research and development of next generation of nonvolatile memory at universities. The design and integration path took into account the restrictions imposed by the available equipment for integrating two discrete processing services. Electrical testing revealed no shorts or opens resulting from misalignment or due to the processing steps. Possibility of multi state operation was discovered in the electrical characterization of Ge_2Se_3/SnSe two terminal devices.

CHAPTER 4: DELTA-SIGMA MODULATION BASED SENSING

It's evident that chalcogenide based resistive nonvolatile phase change memory has the potential to exhibit multi state capability and hence the possibility of storing multiple bits on a single memory cell. The resistance of these states can vary from a few kΩ to several kΩ or even MΩ [2], [5]. Traditional sensing schemes use differential sensing, where the output of an "actual" cell is compared to a "dummy" cell by a differential amplifier to determine the state of the actual memory cell [12], [13]. The differential sensing scheme has major shortcomings; it is sensitive to process variations and noise, and demands wide resistance margins to sense reliably.

This chapter presents the design of four resistive memory sensing circuit topologies employing Delta-Sigma (ΔΣ) modulation. Delta-Sigma modulation (DSM) based sensing schemes can be very practical and robust [14-16] and have the advantage over traditional sensing [17] circuits in being able to rapidly distinguish resistance values (memory states) within a fraction of the actual value being sensed [18]. The Delta-Sigma modulation (DSM) based sensing circuit developed for sensing Phase Change Random Access Memory (PCRAM) employs voltage mode sensing. In voltage mode sensing, the voltage change at the bitline is sensed and used to determine the state of the memory cell connected to the bitline. The sensing circuitry for the chalcogenide based phase change random access memory was designed and fabricated externally to the chip containing the test structures discussed in the previous chapter. Four distinct Delta-Sigma (ΔΣ)

modulation based sensing topologies were developed and fabricated in AMI's C5 process through the MOSIS fabrication service.

Qualitative Description of DSM Sensing Circuit

Figure 4.1 shows an example ΔΣ modulation based sensing circuit. The DSM circuit consists of an integrating capacitor C_{bit} (bitline capacitance), an analog to digital converter in the form of a comparator connected to the bitline and a feedback loop which acts as a digital to analog converter to maintain the bitline at a constant voltage.

The sensing circuit works on the principle of sensing the change in bitline voltage over a period due to current discharge from the sigma capacitor (bitline capacitance) through the memory cell based on its state, while using the feedback loop to maintain the bitline voltage at around a constant value. During this operation the number of times the output of the sense amp goes high (or low) are recorded and used to determine the state of the memory cell.

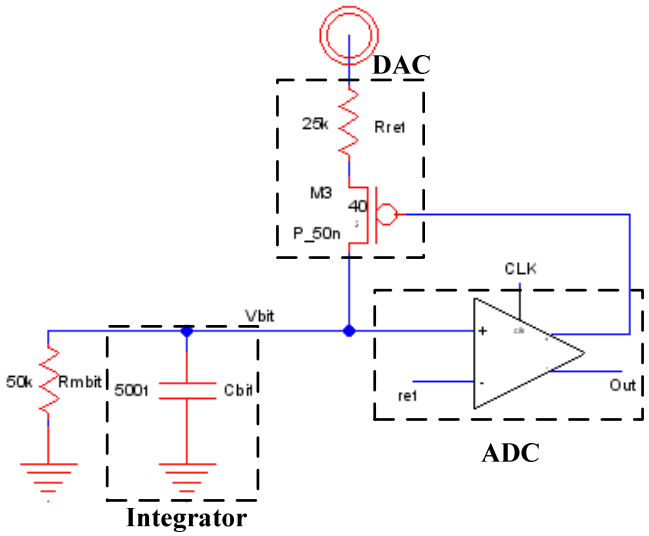


Figure 4.1 Delta-sigma modulation based sensing for resistive memory.

Sensing Operation

The sensing begins with the bitline capacitor C_{bit} being charged to a voltage above the reference voltage (V_{ref}) connected to the comparator's negative terminal. This causes the comparator's output terminal to turn 'high' thus turning OFF the PMOS switch S1, effectively cutting the supply of charge to bitline capacitance through the reference resistor R_{ref}. Now during the sense operation, based on the current state of the memory cell (SET or RESET), the bitline voltage either stays at a constant voltage V_{ref} or discharges to ground through the memory cell. This change in bitline voltage is due to the constant discharge of charge from the bitline capacitance C_{bit} through the memory cell's resistance. Each time the bitline voltage reaches the reference voltage, the feedback loop causes PMOS switch S1 to turn back ON thus causing the sigma capacitor C_{bit} to charge back to a value above the reference voltage. N is recorded as the number of times the comparator is clocked and the number of clock cycles the comparator's output stays low is recorded as M.

Considering the bitline voltage to be V_{bit}, the current sunk by the resistive memory element R_{mbit} is I_{mbit}. The current supplied through the reference resistor R_{ref} is I_{ref}. Then the current supplied to the bitline capacitance C_{bit} is,

$$I_{ref} \cdot \frac{M}{N} \tag{4.1}$$

Since the current supplied to C_{bit} is equal to the current sunk by R_{mbit}, we can write as;

$$I_{mbit} = I_{ref} \cdot \frac{M}{N} \tag{4.2}$$

Now, we can write I_{mbit} as $\frac{V_{bit}}{R_{mbit}}$ and I_{ref} as $\frac{(VDD - V_{bit})}{R_{ref}}$, on average therefore;

$$\frac{V_{bit}}{R_{mbit}} = \frac{M}{N} \cdot \frac{(VDD - V_{bit})}{R_{ref}} \tag{4.3}$$

Since V_{bit} is held at approximately $V_{ref} = \frac{VDD}{2}$

$$R_{mbit} = \frac{N}{M} \cdot R_{ref} \tag{4.4}$$

In a real implementation of the circuit the actual resistance (R_{mbit}) of the memory element is not calculated, instead, a counter is employed to count the comparator output count (M) that is used to charge C_{bit}. This count is compared to a reference count [18] which is usually selected to represent a value between the logic 0 and logic 1 or other levels in multi level cells. Hence a count value greater than the reference count indicates one logic state and a count value less than the reference count indicates another.

DSM Circuit Components and Design Considerations

As seen in Figure 4.1, the DSM circuitry consists mainly of the integrator (C_{bit}), the analog to digital converter (Comparator) and the digital to analog converter (PMOS switch and resistor). The following section describes the design considerations taken into account for the design of these components for four variants of DSM sensing circuit and their effect on sensing.

Integrator

The integrator consists simply of the bitline capacitance of the memory array columnline. Its value depends on process, size of the array and the memory cell size.

Knowing the bitline capacitance prior to the design is very crucial in the design of Delta-sigma Sense Amp (DSSA). The value of bitline capacitance C_{bit} and memory resistance R_{mbit} determines the rate of discharge of charge through the memory bit R_{mbit}. Meanwhile the comparator has to be clocked prior to C_{bit} getting discharged completely to avoid losing the benefit of averaging. For this reason, to determine the minimum clock for the comparator, a minimum value of R_{mbit} is used; since the discharge rate is high for small values of resistance.

Considering the minimum value of memory resistance to be sensed as 10 kΩ, the maximum current that discharges through the memory bit when the bitline voltage (V_{bit}) is held at an average value of 2.5 V is,

$$\mathrm{I_{bit}} = 250\ \mu\mathrm{A} \tag{4.5}$$

The charge stored in the bitline capacitance C_{bit} is,

$$Q_{bit} = C_{bit} \times V_{bit} \tag{4.6}$$

$$T = C_{bit} \times \frac{V_{bit}}{I_{bit}} \tag{4.7}$$

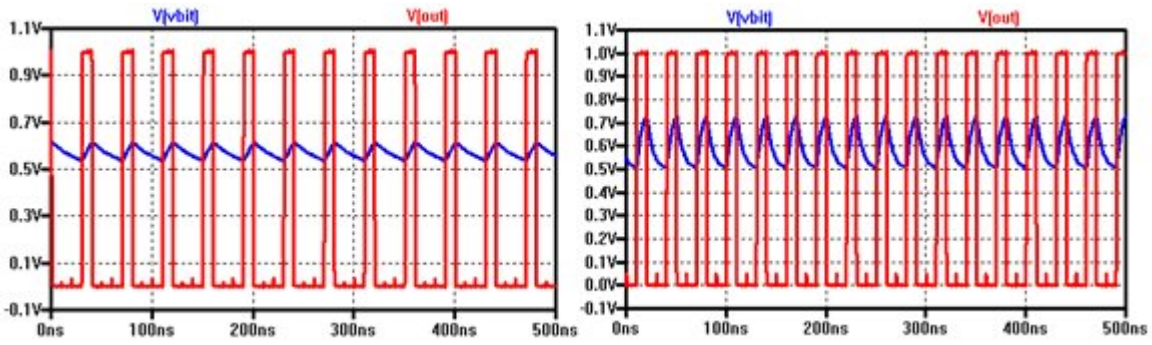
Using Eq. (4.7), Table 4.1 is tablulated showing the discharge times for various bitline capacitances.

Table 4.1 Bitline capacitance discharge times for R_{mbit} = 10 kΩ.

Bitline Capacitance C_{bit}	**Discharge Time T**
1 pF	10 ns
10 pF	100 ns
20 pF	200 ns
50 pF	500 ns

From the values in Table 4.1, for an R_{mbit} of 10 kΩ, when I_{bit} is maximum at 250 μA, if the bitline capacitance is 20 pF the comparator has to be clocked within 200 ns to avoid C_{bit} from discharging completely. Therefore a clock f_{clk}, of 10 MHz with a time period of 100 ns would be more than adequate and fast as well. Generally, the bitline capacitance of memory array is around 3 to 5 pF. Since while testing, an additional 14 pF of capacitance is added due to the analog probe tip on the bitline, the comparator's clock frequency is selected accordingly. While the discharging rate of the capacitor sets the minimum frequency required to clock the comparator, there is no limitation for the maximum clock frequency.

The value of bitline capacitance also has an effect on the bitline swing. This is illustrated in Figure 4.2a and b by simulating the circuit in Figure 4.1. A change in C_{bit} from 500 fF to 100 fF causes the ΔV_{bit} to change from 100 mV to 225 mV.



a) C_{bit} = 500 fF; ΔV_{bit} = 100 mV **b)** C_{bit} = 100 fF; ΔV_{bit} = 225 mV

Figure 4.2 DSM output for various bitline capacitance C_{bit}.

Analog to Digital Converter

Clocked Comparator

The clocked comparator used as an analog to digital converter is a robust design with several advantages. The clocked comparator design shown in Figure 4.3 is highly sensitive to milli-volt level voltage difference on its input terminals and has high gain due to the large voltage drop across the drain to source voltage of the input transistors. The circuit does not possess memory, since prior to the sensing operation all nodes in the circuit are set to known voltages. This design also reduces kickback noise since the inputs are isolated from the output.

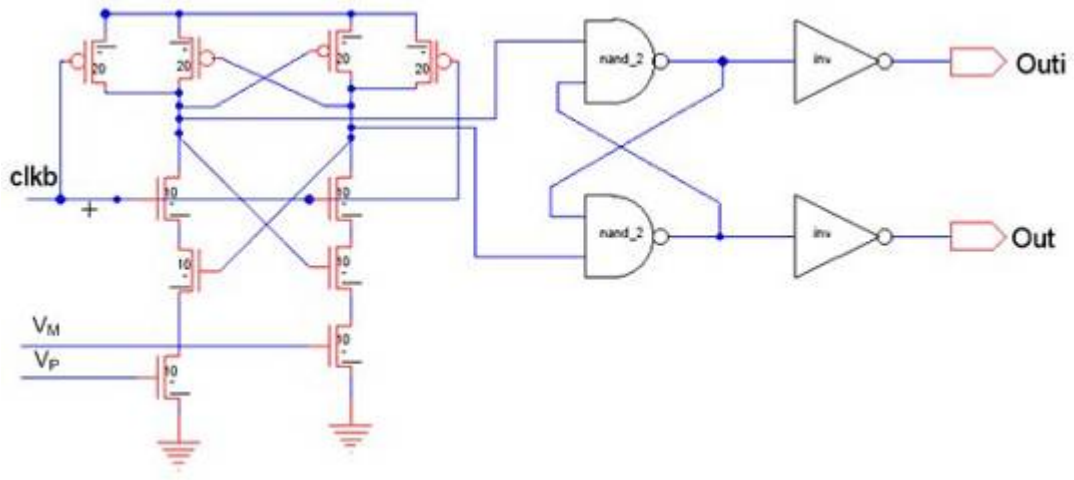


Figure 4.3 Clocked comparator with SR latch output.

The clocked comparator has an output SR latch whose output changes on the rising (or falling) edge of a clock signal. When clock is low, the input to the SR latch is pulled high through the PMOS transistors and thus the output of the SR latch does not change. Once clock goes high, any slight variation at sense-amplifier inputs V_M and V_P are sensed causing the output to register which input is higher.

The main draw back in this circuit is the requirement for input voltage to be above the threshold voltage of the input transistor to turn them ON. This is not a concern in this DSSA design since both the input terminals are expected to be at around 2.5 V, well above the NMOS threshold voltage. The layout of the clocked comparator is shown in Figure 4.4.

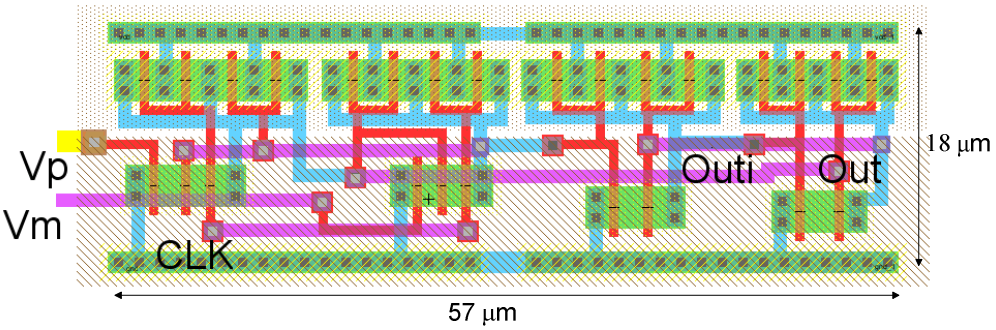


Figure 4.4 Layout of the clocked comparator.

Figure 4.5 shows the simulation results of the comparator used in DSSA. For the simulations, a ramp signal varying from 0 to 5 V is given to the negative input terminal V_M while a sine wave signal from 0 to 5 V is used for the positive input terminal V_P. The output displayed in the below simulations are taken at the output of the SR latch.

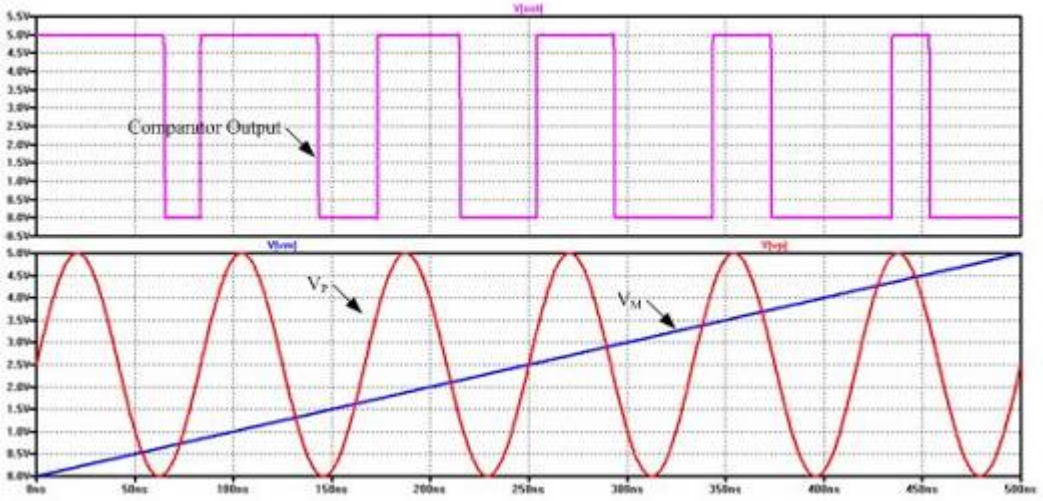


Figure 4.5 Comparator simulation.

Figure 4.6 is used to determine the offset of the comparator design. For this simulation the negative input terminal is held at 2.5 V while the positive input terminal is varied from 2.4 V to 2.6 V. From the simulation result, we see that the comparator switches almost exactly when the V_P reaches 2.5 V thus ensuring the 0 V offset for the comparator. Note that the comparator does not have any transistor mismatch and hence the 0 V offset. A comparator with an intentionally introduced offset will be discussed in subsequent sections.

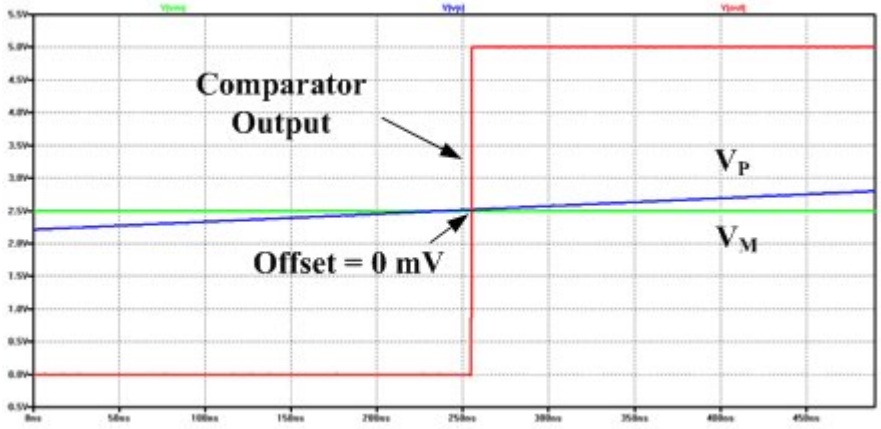


Figure 4.6 Simulating the comparator to determine the offset.

Digital to Analog Converter and Reference Resistor

The digital to analog converter consists of a feedback circuit from the output of the comparator to a PMOS transistor which acts as a switch. The switch, when enabled connects a current source (R_{ref}) to the bitline capacitor C_{bit}. During sensing, the switch is disabled and the bitline capacitance discharges through the memory cell R_{mbit}. Once the voltage across C_{bit} reaches the reference voltage V_{ref}, the feedback loop enables the PMOS switch causing C_{bit} to charge by the current supplied through R_{ref} to a voltage above the reference voltage.

The value of R_{ref} should always be less than the resistance of the memory cell that is being sensed. Using Eq. (4.2) as M value approaches the number of times the comparator is clocked N, the current supplied through the reference resistor I_{ref} becomes equal to the current sunk by the memory cell I_{mbit}. Now, we know that I_{ref} depends on R_{ref} and I_{mbit} depends on R_{mbit}. Hence, we can also state that, as the value of R_{ref} starts to approach the memory cells resistance R_{mbit},the current supplied through the reference resistor I_{ref} becomes equal to current sunk by the memory cell I_{mbit}. This can be used to derive an inverse relationship between the reference resistor R_{ref} and the comparator output count M as shown in Figure 4.7 and Eq. (4.4). We see that as the value R_{ref} approaches R_{mbit} the comparator count value equals the number of times the comparator is clocked. In other words, the comparator output always remains high thus losing the advantage of averaging. For this reason, the reference resistor value must always be less than the memory cell's resistance. A combination of discrete resistors and switched-capacitor resistors are used in the four DSM sensing circuits which will be discussed in the following sections.

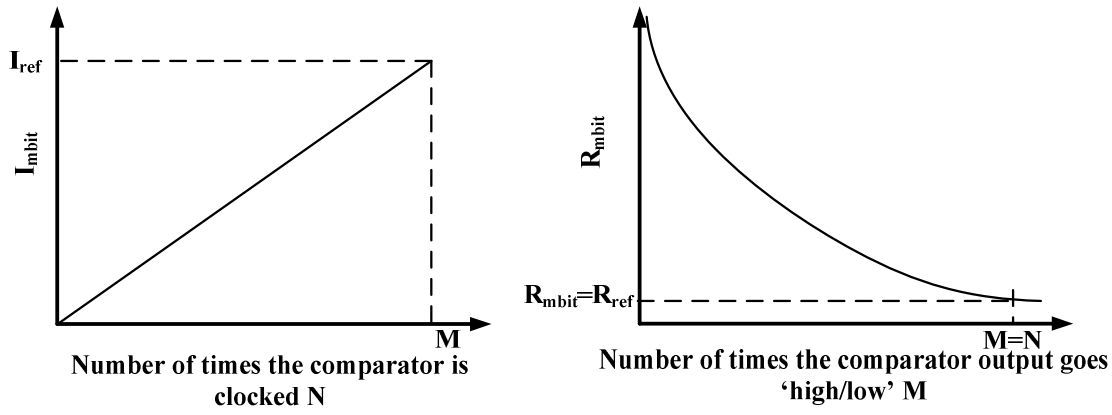


Figure 4.7 Relationship between R_{ref}, I_{mbit} and comparator parameters.

DSM Based Sensing Topologies

Reference Resistor-Based Delta-Sigma Sensing with No Offset

The reference resistor used in the DSM topology can either be a discrete resistor or a switched-capacitor based resistor. This topology uses a discrete resistor to supply charge to the bitline capacitance. The comparator used in this topology has zero offset for switching point voltage. The topology and its associated circuit are shown in Figure 4.8.

Figure 4.8 does not show the sigma capacitor, memory cell or the reference resistor. A discrete reference resistor is connected to the terminal named 'Cup'. Usually the memory cell's resistance is known and the discrete resistor of lesser resistance value is selected accordingly and can be designed on chip. The sigma capacitor is connected externally at the terminal 'bitline' in Figure 4.8. The value of the sigma capacitor represents the bitline capacitance of the memory array the sensing circuit is designed for. The resistance representing the memory bit is also connected externally to the terminal 'bitline' using a discrete resistor. A discrete resistor is used in this design to demonstrate

the flexibility of the DSM topology to various resistance value of the memory cell. A reference voltage source is connected to the VCM terminal.

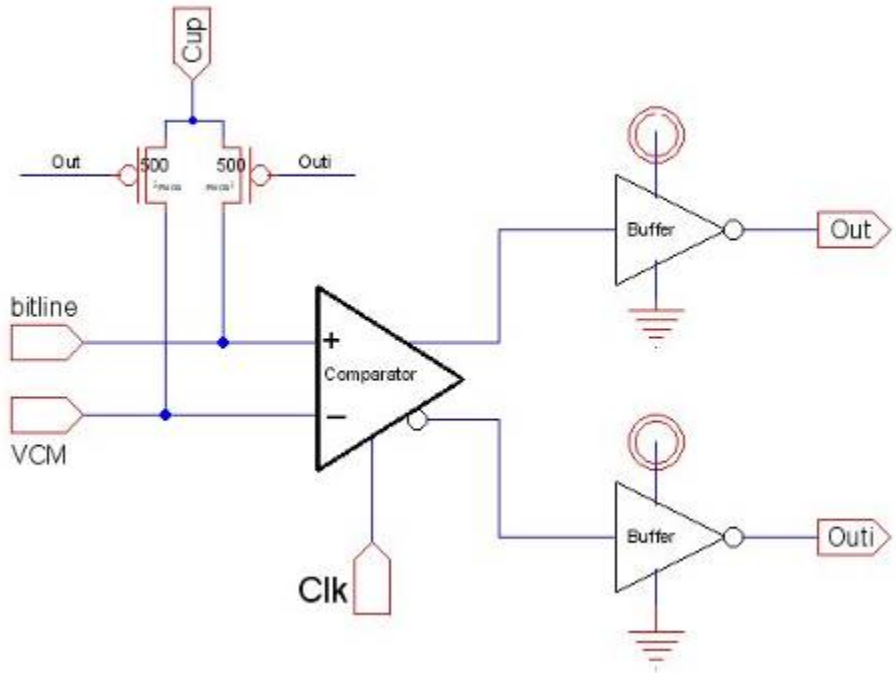


Figure 4.8 Reference resistor-based ΔΣ sensing circuit.

Buffers are designed at the output of the comparator to provide enough drive to retrieve the signals off chip from the bond pads. The switch S2 in Figure 4.8 is used to provide a path for the current from VDD, so that the ref node indicated in the figure does not charge up to an unknown value when S1 is OFF. In the absence of switch S2, when S1 is OFF, ref node is charged up to an unknown value. This charge is dumped on the bitline when S1 turns ON, causing a sudden increase in the bitline voltage rather than a gradual raise.

Based on earlier discussion on the operation of DSM, for the average voltage on the sigma capacitor to remain constant, the average amount of charge entering the sigma

capacitor C_{bit} in one clock cycle T ($1/f_{clk}$), $Q_{ref,}$ should be equal to the average amount of charge sunk by the memory cell Q_{mbit}.

$$Q_{mbit} = Q_{ref} \tag{4.10}$$

If M is the number of clock cycles the comparator output 'Out' stays high out of N number times it is clocked, the relationship between charge supplied to the bitline capacitance Q_{ref} and the charge sunk by the memory cell Q_{mbit} is given by,

$$Q_{mbit} = Q_{ref} \cdot (M/N) \tag{4.11}$$

$$I_{mbit} \cdot T = I_{ref} \cdot (M/N) \cdot T \tag{4.12}$$

Hence the average current supplied to the sigma capacitor I_{ref} is equal to the average current sunk by the memory cell I_{mbit}.

$$I_{mbit} = I_{ref} \cdot (M/N) \tag{4.13}$$

$$(VDD/(2 \cdot R_{mbit})) = (VDD/(2 \cdot R_{ref})) \cdot (M/N) \tag{4.14}$$

$$R_{mbit} = R_{ref} \cdot (N/M) \tag{4.15}$$

The ratio of the number of clock cycles the comparator output goes high M, to the number of times the comparator is clocked N, gives the ratio of the reference resistance used to the resistance of the memory cell.

$$\frac{M}{N} = \frac{R_{ref}}{R_{mbit}} \tag{4.16}$$

The least resistance that can be measured using this topology is limited only by the reference resistor as explained in earlier sections. The maximum resistance that can be sensed depends on the sense time. As the resistance of the memory cell increases, the discharge time of the bitline capacitance increases. Thus the comparator output stays low

for an increased number of clock cycles requiring longer sense time for higher values of R_{mbit}.

The minimum voltage on the bitline is *VDD*/2. The maximum voltage and bitline is *VDD*/2 + $\Delta V_{bit.}$ The maximum variation in bitline voltage ΔV_{bit} is given by,

$$\Delta V_{bit} \cdot C_{bit} \leq Q_{ref} \tag{4.17}$$

$$\Delta V_{bit} \cdot C_{bit} \leq I_{ref} \cdot T \tag{4.18}$$

$$\Delta V_{bit} \leq \frac{VDD}{2 \cdot R_{ref} \cdot C_{bit} \cdot f_{clk}} \tag{4.19}$$

Figure 4.9 shows the simulation result for reference resistor-based DSM sense amp without comparator offset. Figure 4.10 shows the plot for actual resistor used to model the memory bit's resistance versus sensed resistance from the DSM sense amplifier.

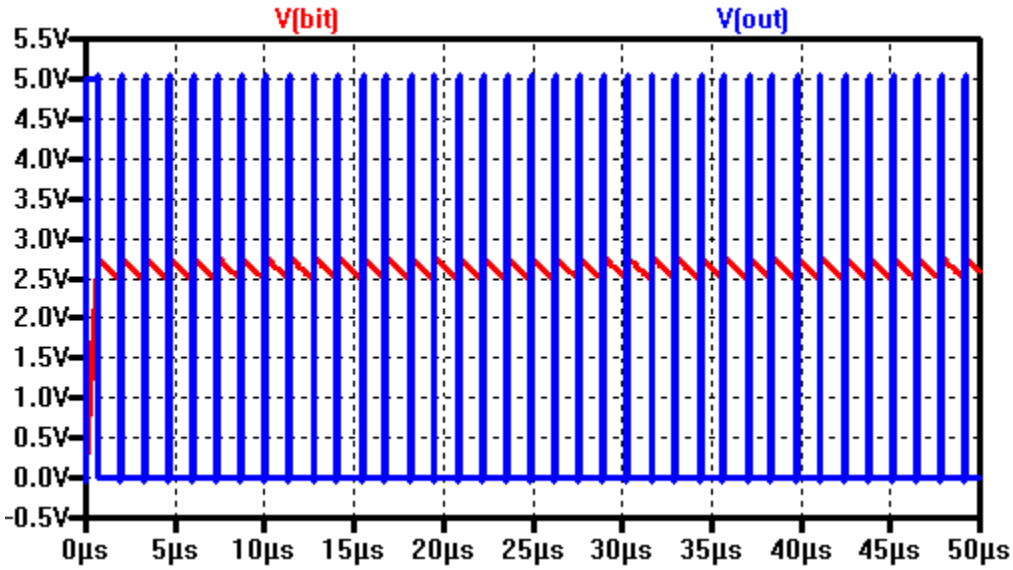


Figure 4.9 Simulation result for reference resistor-based DSM sense amp without comparator offset.

Table 4.2 Reference Resistor-based ΔΣ Sense amp with no offset simulation results.

Memory Cell Resistance (kΩ)	Comparator Output Count M	Calculated Resistance (kΩ)
10	250	10
20	143	17
30	100	25
40	77	32
50	63	40
60	52	48
70	45	56
80	38	66
90	35	71
100	33	76
110	29	86
120	26	96
130	25	100
140	22	114
150	21	119
160	20	125
170	19	132
180	18	139
190	17	147
200	16	156

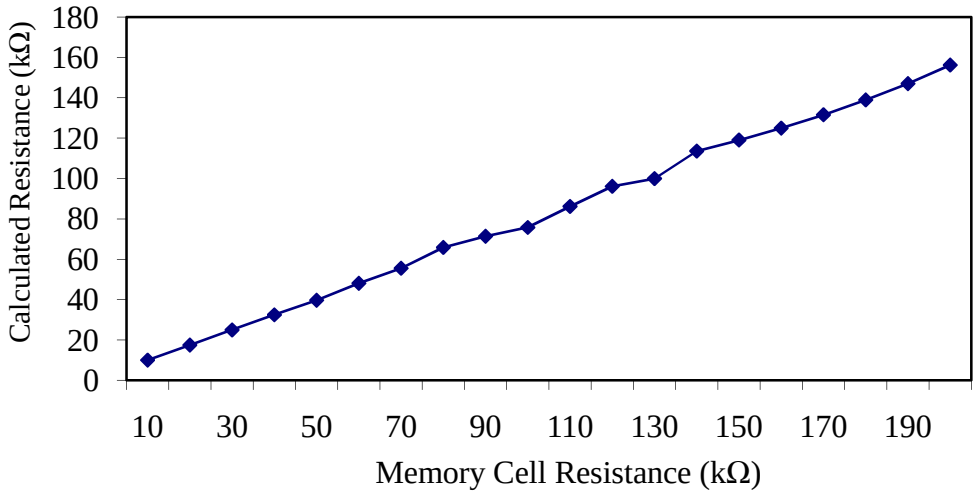


Figure 4.10 Calculated resistances Vs Memory cell resistance for discrete reference resistor-based ΔΣ sense amp without offset.

Reference Resistor-Based Delta-Sigma Sensing with Offset

The voltage across the memory cell was 2.5 V in DSSA circuit topology discussed above. This voltage can sometimes cause the memory cell to switch state based on its threshold voltage as discussed in chapter 2. Minimizing the voltage across the memory cell reduces the stress across the memory element, thus avoiding the memory cell from switching state [19]. To reduce the voltage across the memory cell, a comparator with a built in offset on its reference terminal can be used. This helps in minimizing the number of reference voltages used in the sensing circuit. The comparator designed for this sensing circuit uses only *VDD* and *VDD*/2 as reference voltage and uses a built in offset to reduce the stress across the memory cell.

To add an offset to the comparator design, the size of the transistor on the reference terminal or the negative input terminal V_M is made bigger than the positive input terminal V_P. This imbalance requires the voltage on the positive terminal V_P, to exceed $V_M + V_{OS}$ for the comparator output to switch, where V_{OS} is the offset of the comparator.

The addition of this offset to the comparator causes the voltage on the bitline to remain at an average value of $V_{ref} + V_{OS}$ due to feedback action from the comparator and the PMOS switch. Figure 4.11 shows the comparator simulation to determine the offset. From the simulation we see that comparator output switches state when the positive input terminal V_P is 120 mV above the negative input terminal V_M. Since the memory cell is connected between bitline and V_{ref}, the average voltage across the memory cell is reduced to V_{OS}, thus reducing the stress across the cell.

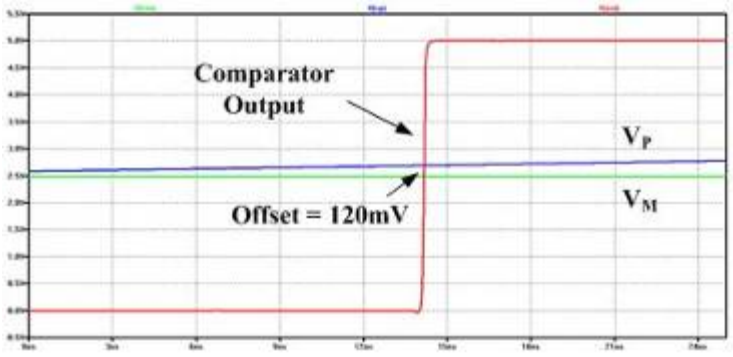


Figure 4.11 Simulation to determine comparator offset.

The main difference in this topology from the previous one in Figure 4.8 is the presence of an offset in the comparator and the reduction of the voltage across the memory cell from *VDD*/2 to V_{OS}.

The equations governing the operation of this topology are given below. Charge is supplied to the sigma capacitor for M clock cycles out of N; hence the current through the memory cell R_{mbit} is given as,

$$\frac{V_{os}}{R_{mbit}} = \frac{\left(VDD - \left(VDD/2 + V_{os}\right)\right)}{R_{ref}} \cdot \left(M/N\right) \qquad 4.20$$

$$R_{mbit} = R_{ref} \cdot \left(V_{os} \middle/ \left(VDD/2 - V_{os}\right)\right) \cdot \left(N/M\right) \qquad 4.21$$

The minimum voltage on the bitline is *VDD*/2 + V_{OS}. The maximum voltage and bitline is *VDD*/2 + V_{OS} + $\Delta V_{bit..}$ The maximum variation in bitline voltage ΔV_{bit} is given by,

$$\Delta V_{bit} \cdot C_{bit} \le Q_{ref} \qquad 4.22$$

$$\Delta V_{bit} \cdot C_{bit} \le I_{ref} \cdot T \qquad 4.23$$

$$\Delta V_{bit} \le \frac{\left(VDD/2 - V_{os}\right)}{R_{ref} \cdot C_{bit} \cdot f_{clk}} \qquad 4.24$$

Figure 4.12 shows the simulation result for reference resistor-based DSM sense amp with comparator offset. Figure 4.13 shows the plot for actual resistor used to model the memory bit's resistance versus sensed resistance from the DSM sense amplifier.

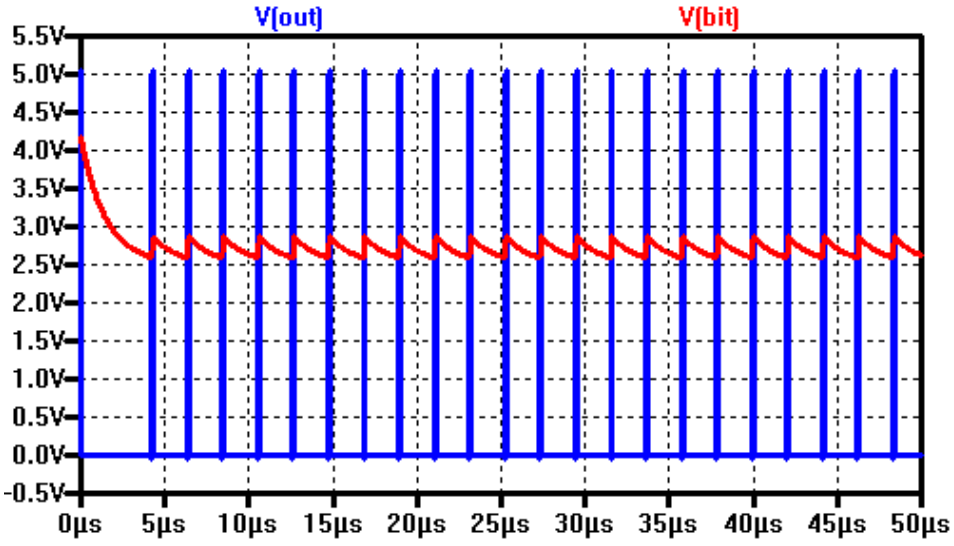


Figure 4.12 Simulation result for reference resistor-based DSM sense amp with comparator offset.

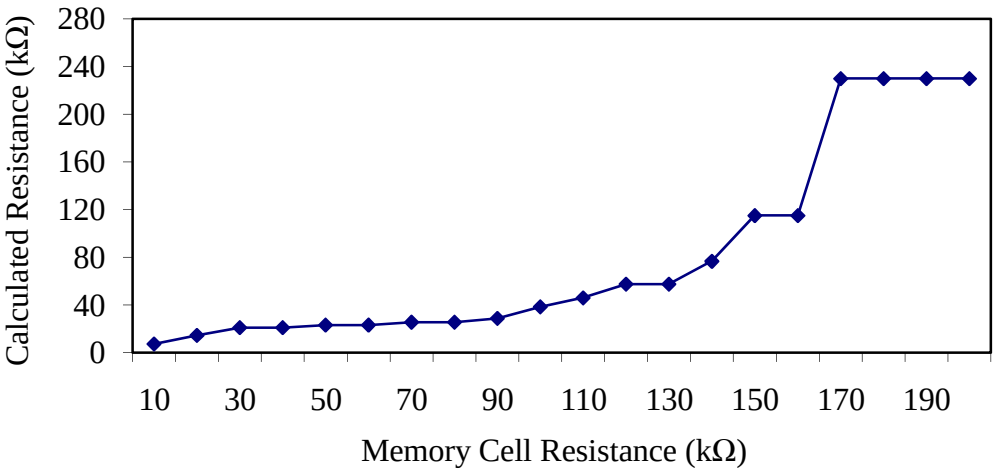


Figure 4.13 Calculated resistances Vs Memory cell resistance for discrete reference resistor-based ΔΣ sense amp with offset.

Table 4.3 Reference Resistor-based ΔΣ Sense amp with offset simulation results.

Memory Cell Resistance (kΩ)	Comparator Output Count M	Calculated Resistance Using Equation (kΩ)	Calculated Resistance Using Ratio (kΩ)
10	32	4	7
20	16	8	14
30	11	11	21
40	11	11	21
50	10	13	23
60	10	13	23
70	9	14	26
80	9	14	26
90	8	16	29
100	6	21	38
110	5	25	46
120	4	32	58
130	4	32	58
140	3	42	77
150	2	63	115
160	2	63	115
170	1	126	230
180	1	126	230
190	1	126	230
200	1	126	230

Switched-Capacitor Resistor-Based Delta-Sigma Sensing with No Offset

The simple reference resistors used in the first two topologies have the disadvantage of restricting the flexibility for tuning the reference resistance value once they are designed on chip. A switched-capacitor resistor built on chip has the flexibility to change the resistance value by varying the clock supplied to it.

The switched-capacitor resistor circuit used in this topology is shown in Figure 4.14. The clock signals given to transistors M1 and M2 are two out of phase non-overlapping clock signal [20] with frequency f_{clk} and period T.

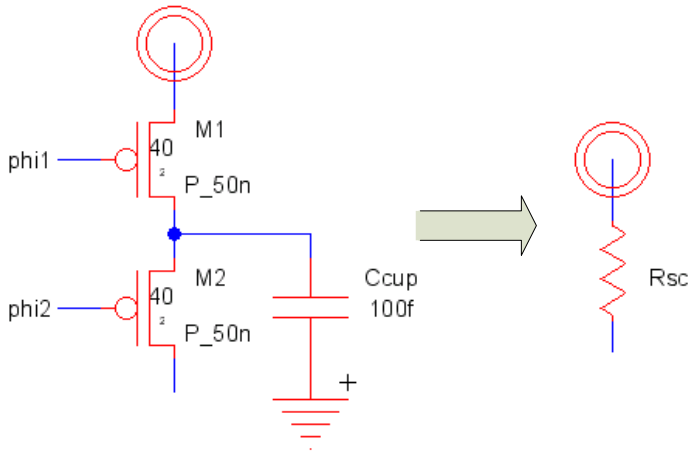


Figure 4.14 Switched-capacitor resistor used in ΔΣ sensing circuit.

Now, considering the case when Φ1 is low and S1 is closed, the capacitor C_{CUP} is charged to *VDD*. The charge stored in the capacitor during this period is,

$$Q_{CUP1} = C_{CUP} \cdot VDD \tag{4.25}$$

When S1 is open and S2 is closed, the charge stored in the capacitor is,

$$Q_{CUP2} = C_{CUP} \cdot \left(\frac{VDD}{2} + V_{THP} \right) \tag{4.26}$$

It is important that M1 and M2 are not turned on at the same time. This is because we never want to connect the bitline directly to *VDD*.

The net charge on C_{CUP} is given by,

$$Q_{CUP} = C_{CUP} \cdot \left(VDD - \frac{VDD}{2} - V_{THP} \right) \tag{4.27}$$

This charge is allowed to flow into the sigma capacitor C_{bit} only when M3 is switched on, which is M times out of N clock cycles. Hence the average current flowing into the bitline capacitor is given by,

$$I_{avg} = \frac{Q_{CUP}}{T} \cdot \frac{M}{N} \tag{4.28}$$

Considering the switched-capacitor resistor's resistance to be R_{SC}, the average current flowing into the bilitne capacitance C_{bit} is,

$$I_{avg} = \frac{VDD - VDD/2 - V_{THP}}{R_{SC}} \tag{4.29}$$

Substituting Eq. (4.28) in (4.29), we get

$$R_{SC} = \frac{1}{C_{CUP} \cdot f} \cdot \frac{N}{M} \tag{4.30}$$

With M3 always enabled, the resistance of the switched-capacitor is,

$$R_{SC} = \frac{1}{C_{CUP} \cdot f} \tag{4.31}$$

The two non-overlapping clocks are generated from a non-overlapping clock generator circuit shown in Figure 4.15. The clock signals Φ1 and Φ2 generated from this circuit is shown in Figure 4.16. The period of dead time between the two clock signals transitioning from high to low is labeled Δ, and is show in the figure. The value of Δ is set by the delay through the inverter connected to the clock signal *Clk*. The buffers connected at the output of the circuit are to provide sharp transitioning clock signals.

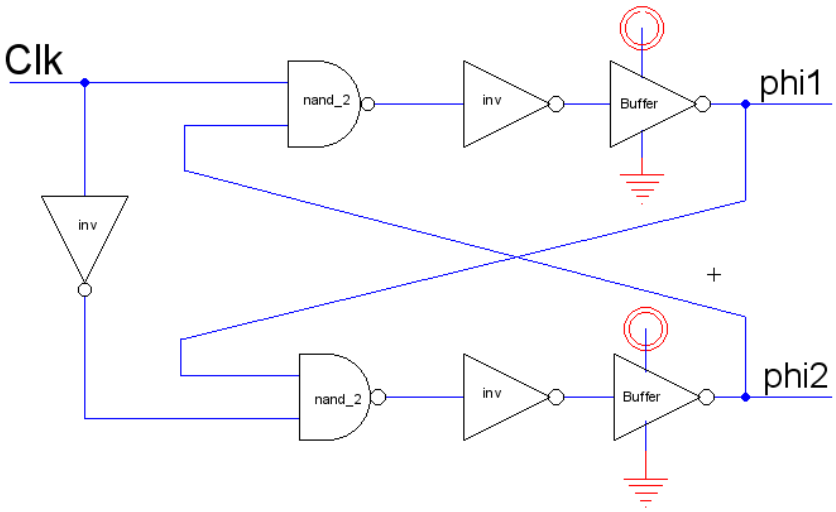


Figure 4.15 Non-overlapping clock generator circuit.

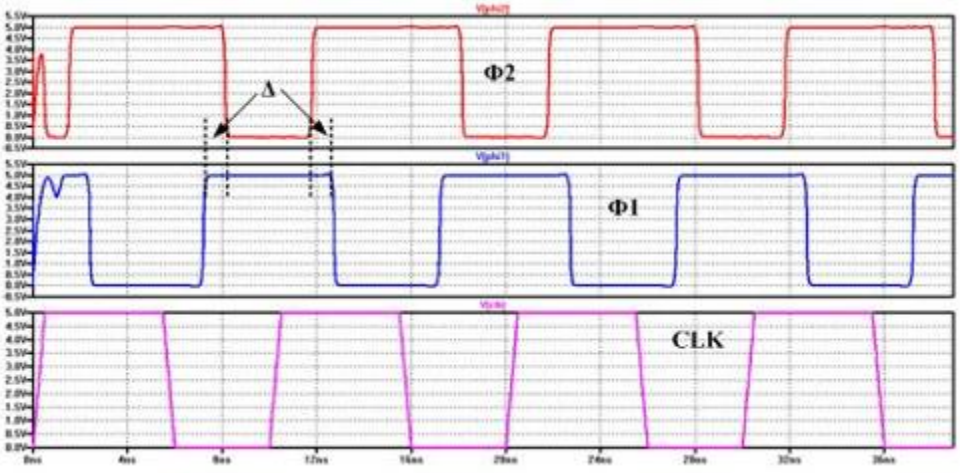


Figure 4.16 Non-overlapping clock signals.

The switched-capacitor resistor-based DSM sensing topology is shown in Figure 4.17. The operation of this sensing circuit is similar to the topologies discussed in the previous sections. When Φ1 is low charge is stored in C_{CUP} from *VDD*. As the charge on the bitline is sunk through the memory cell, every time the value of the bitline voltage reaches $V_{ref,}$ the switch S1 turns ON. When Φ2 goes high now, the charge on C_{CUP} is dumped to the bitline capacitance $C_{bit,}$ thus increasing the bitline voltage to Vref+ΔV_{bit}.

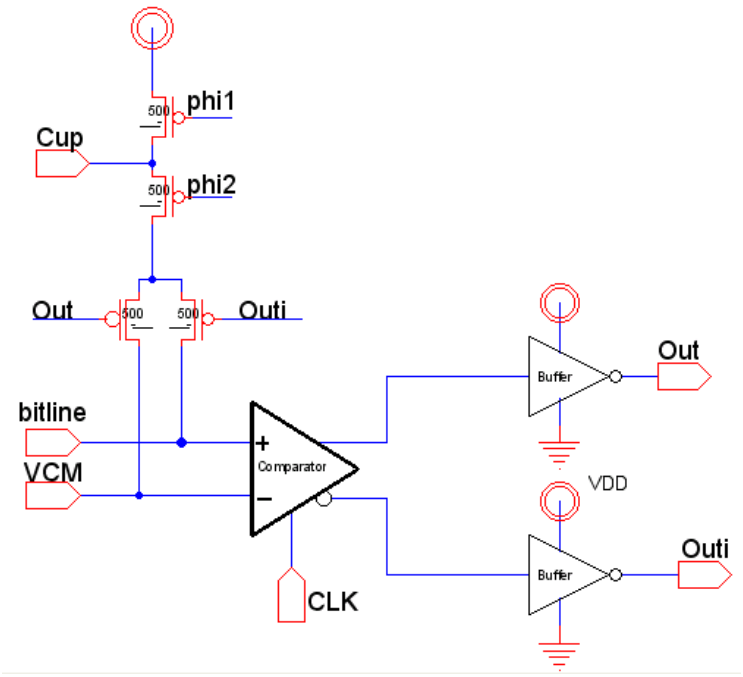


Figure 4.17 Switched-capacitor resistor-based DSM sensing circuit.

The current supplied through the switched-capacitor resistor is equal to the current sunk by the memory cell. Hence,

$$V_{ref}/R_{mbit} = \left(Q_{cup}/T\right)\cdot\left(M/N\right) \qquad 4.32$$

$$\left(VDD/\left(2\cdot R_{mbit}\right)\right) = C_{cup}\cdot\left(VDD - VDD/2\right)\cdot\left(1/T\right)\cdot\left(M/N\right) \qquad 4.33$$

$$R_{mbit} = \left(1/\left(f_{clk}\cdot C_{cup}\right)\right)\cdot\left(N/M\right) \qquad 4.34$$

The following equations are used to determine the maximum bitline variation ΔV_{bit}.

$$C_{cup}\cdot\left(VDD - VDD/2\right) = \Delta V_{bit}\cdot\left(C_{cup} + C_{bit}\right) \qquad 4.35$$

$$\Delta V_{bit} = \left(C_{cup}/\left(C_{cup} + C_{bit}\right)\right)\cdot\left(VDD/2\right) \qquad 4.36$$

Figure 4.18 shows the simulation result for switched-capacitor resistor-based DSM sense amp without comparator offset. Figure 4.19 shows the plot for actual resistor

used to model the memory bit's resistance versus sensed resistance from the DSM sense amplifier.

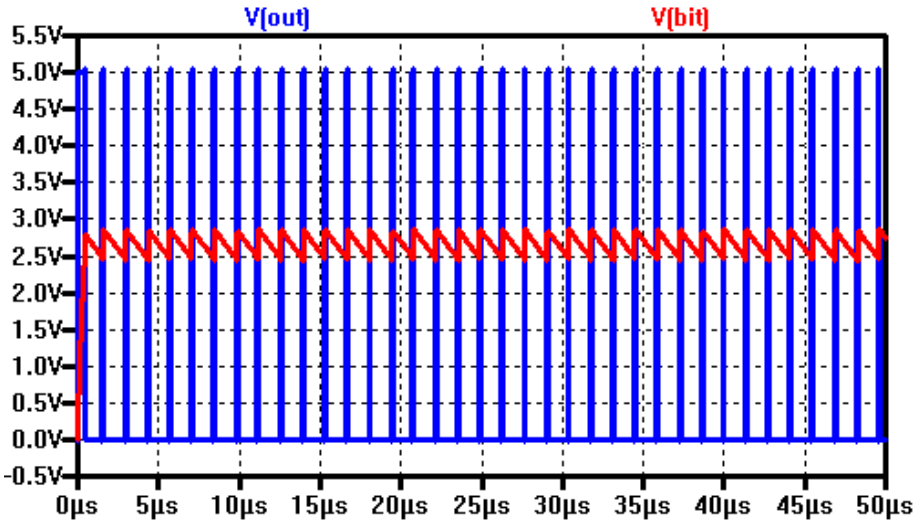


Figure 4.18 Simulation result for switched-capacitor resistor-based DSM sense amp without comparator offset.

Table 4.4 Switched-capacitor resistor-based ΔΣ sense amp without offset simulation results.

Memory Cell Resistance (kΩ)	Comparator Output Count M	Calculated Resistance (kΩ)
108	132	105
147	100	139
205	73	190
248	62	224
298	51	272
350	44	315
403	39	356
458	35	397
497	32	434
560	29	479
620	26	534
1000	17	817
1500	11	1263
2400	7	1984
4100	4	3472

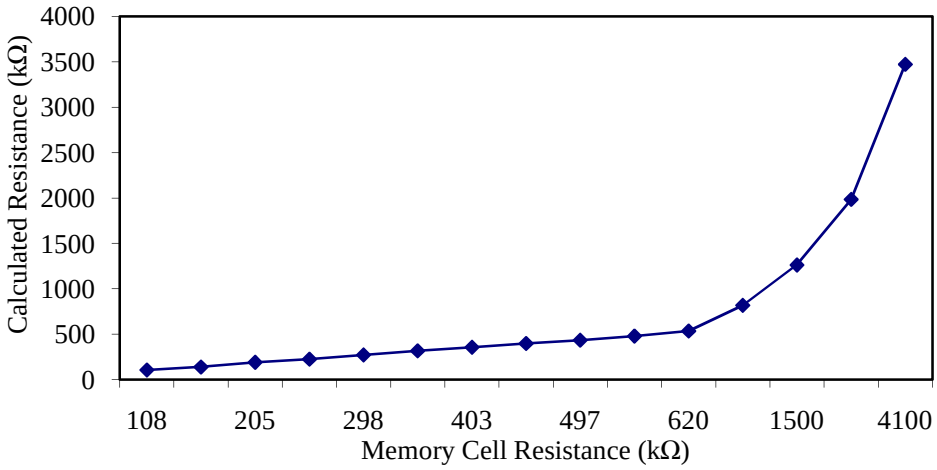


Figure 4.19 Calculated resistances Vs Memory cell resistance for switched-capacitor resistor-based ΔΣ sense amp without offset.

Switched-Capacitor Resistor-Based Delta-Sigma Sensing with Offset

The switched-capacitor based DSM with offset has the flexibility of varying the value of the reference resistor as in the previous DSM topology. This topology also reduces the stress across the memory cell due to the comparator offset as discussed in the sensing topology "Reference resistor-based Delta-Sigma sensing with offset". This DSM topology uses the comparator with the built in offset shown in Figure 4.11 along with a switched-capacitor resistor as the reference resistor. The comparator has a 120 mV offset which sets the voltage across the memory cell to 120 mV instead of 2.5 V, thus reducing the stress across the memory bit and avoiding unintentional program/erase operation.

The equations for this topology are similar to the topology "Reference resistor-based Delta-Sigma sensing with offset". The only difference being the reference resistor is replaced with a switched-capacitor resistor R_{SC} with a value derived in Eq. (4.31),

Substituting Eq. (4.31) in place of R_{ref} in Eq. (4.21) gives,

$$\frac{V_{os}}{R_{mbit}} = \frac{\left(VDD - \left(VDD/2 + V_{os}\right)\right)}{1/C_{CUP} \cdot f} \cdot \left(M/N\right) \tag{4.37}$$

$$R_{mbit} = \left(1/C_{cup} \cdot f\right) \cdot \left(V_{os}/\left(VDD/2 - V_{os}\right)\right) \cdot \left(N/M\right) \tag{4.38}$$

The following equations are used to determine the maximum bitline variation ΔV_{bit}.

$$C_{cup} \cdot \left(VDD - VDD/2 - V_{OS}\right) = \Delta V_{bit} \cdot \left(C_{cup} + C_{bit}\right) \tag{4.39}$$

$$\Delta V_{bit} = \left(C_{cup}/\left(C_{cup} + C_{bit}\right)\right) \times \left(VDD/2 - V_{OS}\right) \tag{4.40}$$

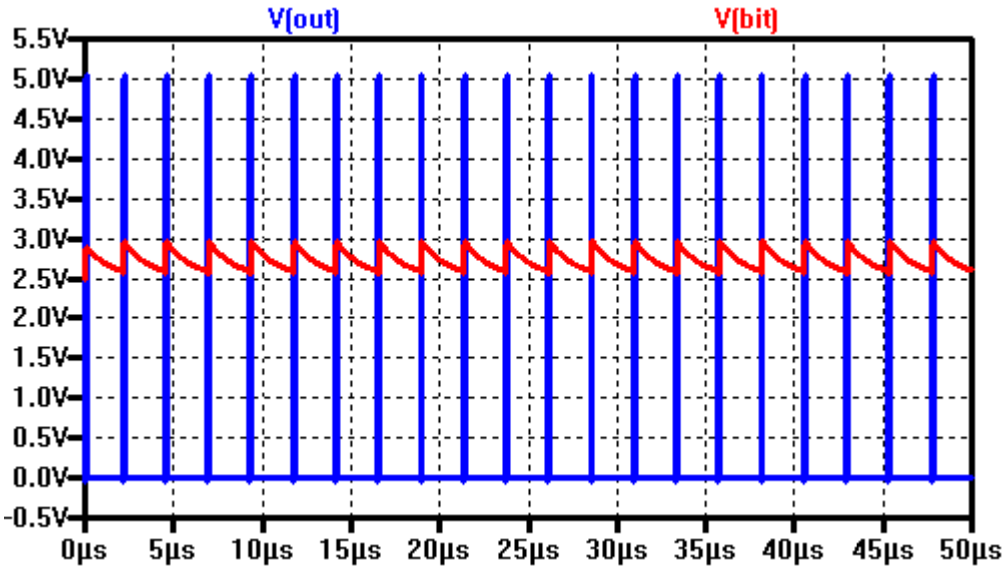


Figure 4.20 Simulation result for switched-capacitor resistor-based DSM sensing circuit with offset.

Table 4.5 Switched-capacitor resistor-based ΔΣ sense amp with offset simulation results.

Memory Cell Resistance (kΩ)	Comparator Output Count M	Calculated Resistance Using Equation (kΩ)	Calculated Resistance Using Ratio (kΩ)
10	127	1	10
20	75	2	18
30	52	3	26
40	40	4	32
50	30	6	37
60	25	7	43
70	20	9	53
80	19	9	59
90	18	9	63
100	16	11	71
110	15	11	77
120	13	13	77
130	13	13	91
140	11	15	91
150	11	15	100
160	10	17	100
170	10	17	111
180	9	19	111
190	8	21	125
200	8	21	125

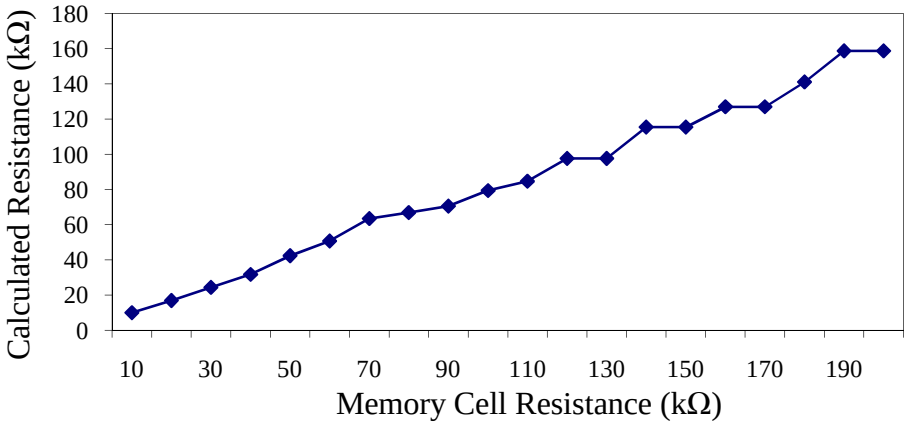


Figure 4.21Calculated resistances Vs Memory cell resistance for switched-capacitor resistor-based ΔΣ sense amp with offset.

Summary

Four Delta-Sigma Modulation topologies design have been presented. DSM based sense amps use averaging to determine the state of a memory cell. The accuracy of the sense amp increases due to this averaging effect removing the effects of unwanted signals like noise. Wide range of resistances from a few kΩ to hundreds of MΩ can be sensed using these four sensing topologies with a high level of accuracy. The comparator design for the DSM sense amp was discussed and feasibility and drawbacks were analyzed. The sense amps were designed with discrete resistors or switched-capacitor resistors in combination with comparator designed with and without an offset. The DSM sense amp with a switched-capacitor resistor with a built in offset in the comparator allows the most flexibility during operation. Also, knowing the bitline capacitance prior to design is a very important consideration in the design of the DSM sense amp.

CHAPTER 5: CHIP TESTING

A set of two chips were designed to demonstrate the PCRAM operation principle discussed in Chapter 2 and 3. Chips were also fabricated to demonstrate the four DSM topologies explained in Chapter 4. The chips were designed using Electric VLSI Design System and fabricated in AMI C5N process using MOSIS fabrication service as mentioned in the earlier chapters. The first of the PCRAM chips has been fabricated and successfully tested at Boise State University. The second PCRAM chip has been fabricated is currently being tested. The second chip differs from the first chip mainly in the fabrication of the bottom electrode for the memory bits, which were made in Tungsten instead of Copper. Also the bottom electrode sizes were a constant 0.6 μm by 0.6 μm due to the limitations of AMI C5N fabrication service for the layout of 'vias'. The number of test structures in the second chip was also reduced to increase the size of the alignment marks and increase the tolerance for misalignments discussed in chapter 3.

Layout, Chip Micrograph and Test Results

NASA Chip 1

The following information gives more details about NASA chip1. The chip has a dimension of 2.95 mm by 2.95 mm. Four chips were fabricated at IML for a combination of memory stacks of Ge_2Se_3-SnTe and Ge_2Se_3-SnSe. Figure 5.1 shows the layout view of

the chip with the various test structures and their associated site numbers. Table 5.1 gives details about the various test structures along with the site numbers on the die. The chip micrograph is shown in Figure 5.2.

- **Fabrication Service**: MOSIS & Idaho Micro Fabrication Lab (BSU)
- **Process**: AMI C5N
- **Design Rules**: SCMOS_SUBM [3]
- **Lambda**: 0.30
- **Feature size**: 0.60
- **No. of Layers of Metal**: 3
- **Voltage**: 5
- T**ool**: Electric VLSI Design

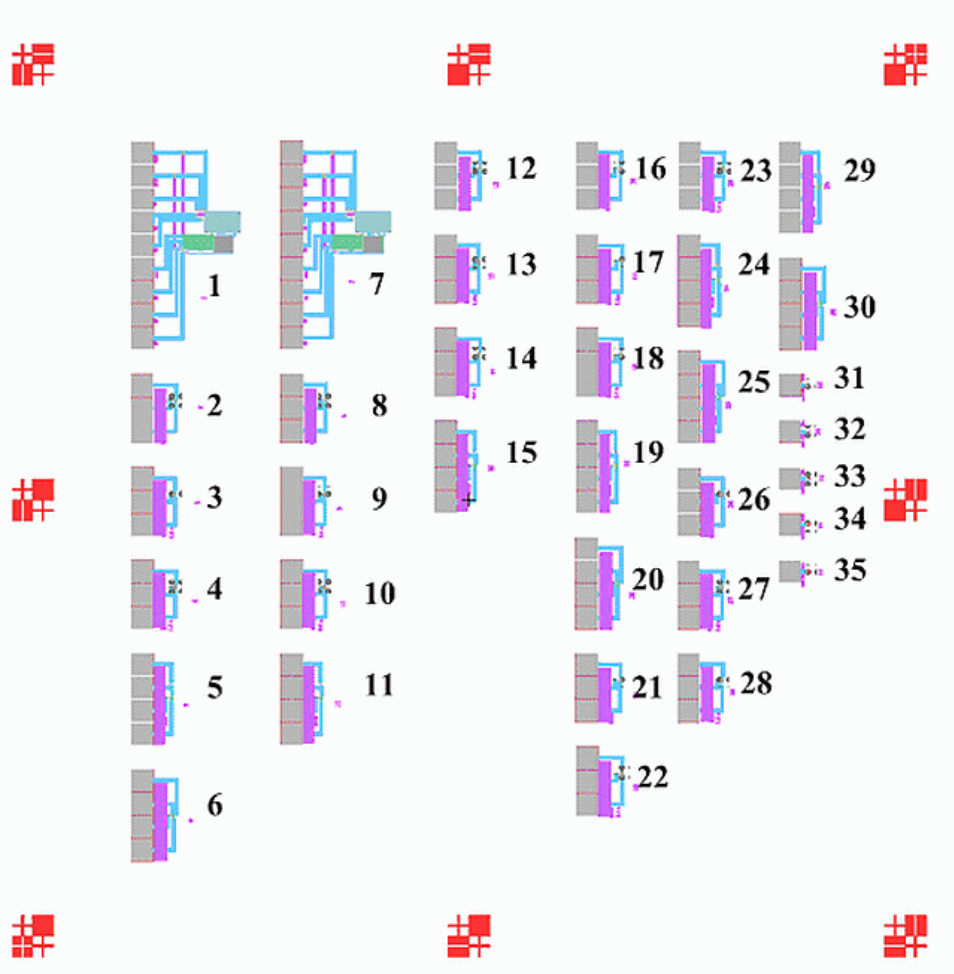


Figure 5.1 Layout view of NASA Chip 1.

Table 5.1 Description of the test structures along with their site number on the die.

Test Structure	Size	Site Location	Number of Test Structures	Comment
Array Test Structure	32/2	1,7	2	32/2 Mbit
NMOS MBIT	32/2	2,8,12	3	Std. Via Size (1.8u)
	32/2	3,9,13	3	Via Size 3.6u
	32/2	4,10,14	3	Via Size 5.4u
NMOS Transistor	32/2	5,11,15	3	Access Transistor
PMOS Transistor	24/2	6	1	Access Transistor
NMOS MBIT	24/2	16	1	Std. Via Size (1.8u)
	24/2	17	1	Via Size 3.6u
	24/2	18	1	Via Size 5.4u
NMOS Transistor	24/2	19	1	Access Transistor
PMOS Transistor	24/2	20	1	Access Transistor
NMOS MBIT	28/2	21	1	Std. Via Size (1.8u)
	28/2	22	1	Via Size 3.6u
	28/2	23	1	Via Size 5.4u
NMOS Transistor	28/2	24	1	Access Transistor
PMOS Transistor	28/2	25	1	Access Transistor
NMOS MBIT	40/2	26	1	Std. Via Size (1.8u)
	40/2	27	1	Via Size 3.6u
	40/2	28	1	Via Size 5.4u
NMOS Transistor	40/2	29	1	Access Transistor
PMOS Transistor	40/2	30	1	Access Transistor
Resistor Bit Test Structure	1.8u	31,32	2	Metal 3 layer size
	3.6u	33	1	Metal 3 layer size
	3.6u	34	1	Metal 3 layer size
	5.4u	35	1	Metal 3 layer size

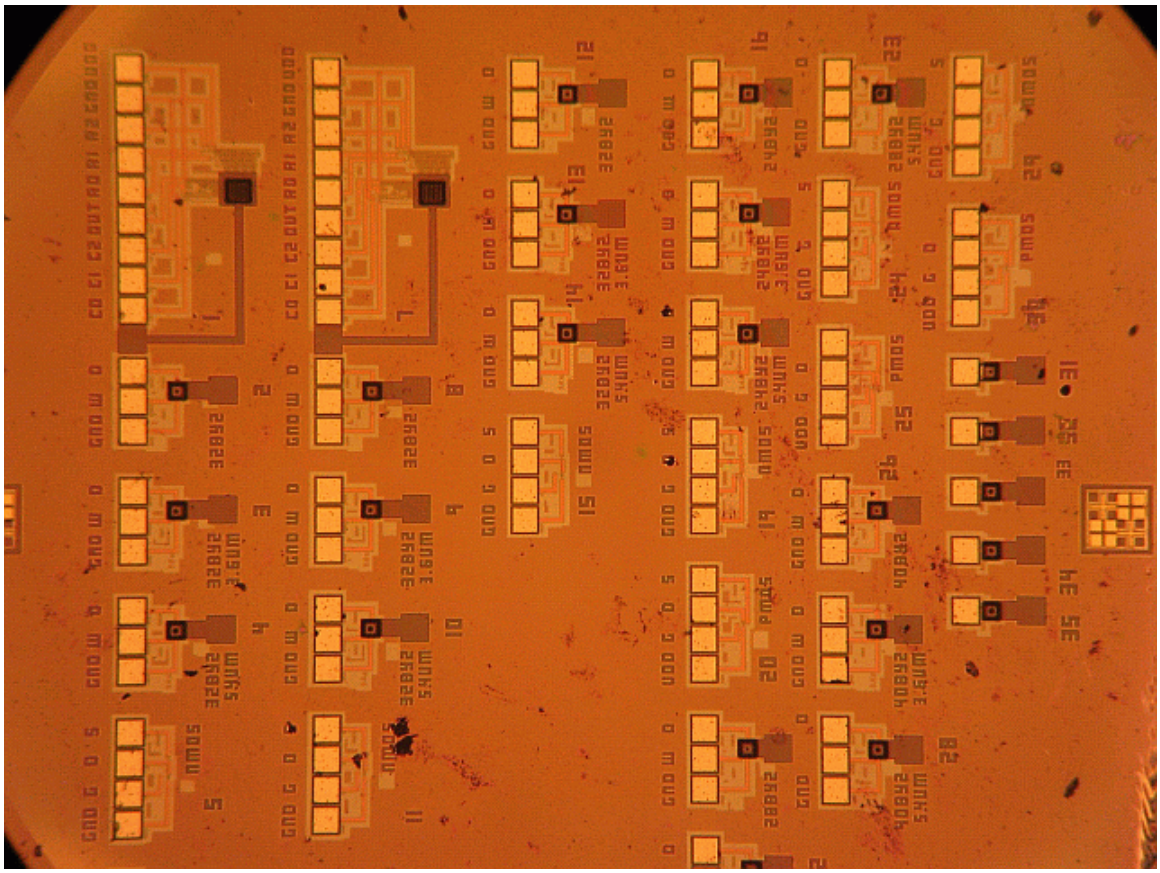


Figure 5.2 Micrograph of NASA Chip 1.

The individual test structures on the NASA Chip 1 are shown in Figures 5.3 to 5.6. The site numbers associated with the test structures and other layout texts seen in the micrograph were fabricated on chip at Idaho Micro fabrication Lab during the deposition of chalcogenide and Tungsten.

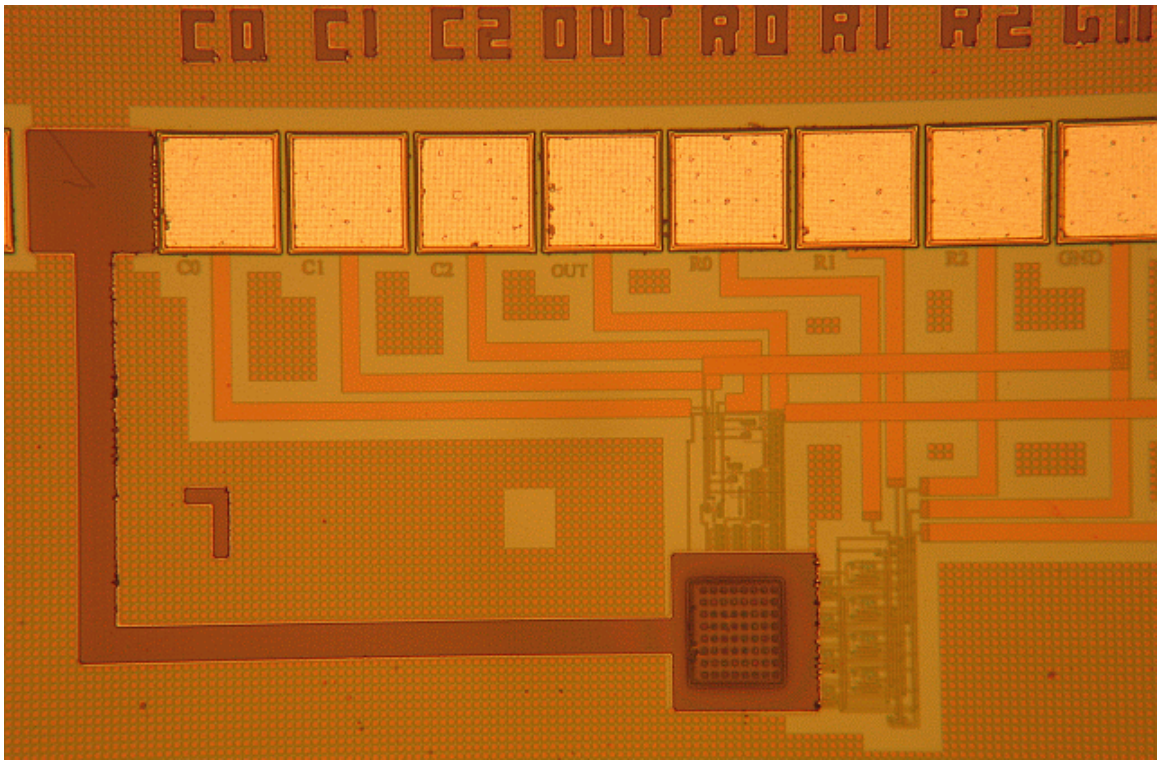


Figure 5.3 Micrograph of memory array.

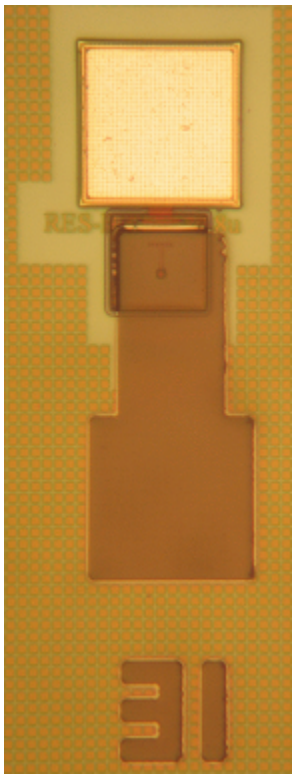


Figure 5.4 Micrograph of resistor bit.

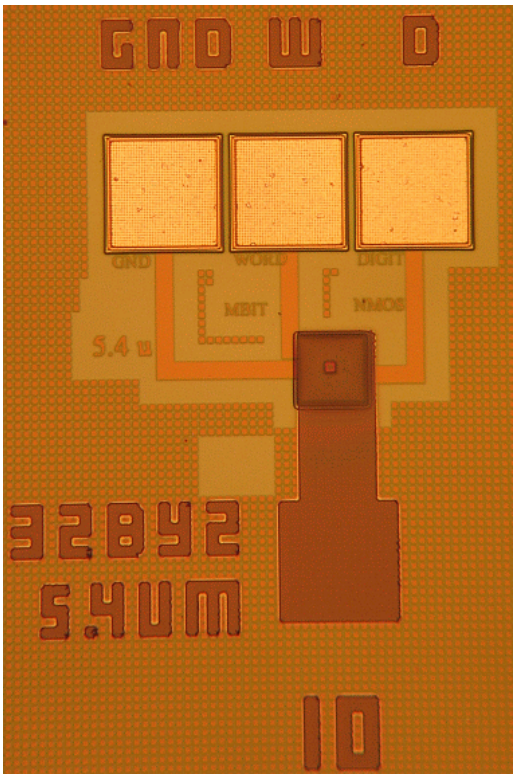


Figure 5.5 Micrograph of Mbit.

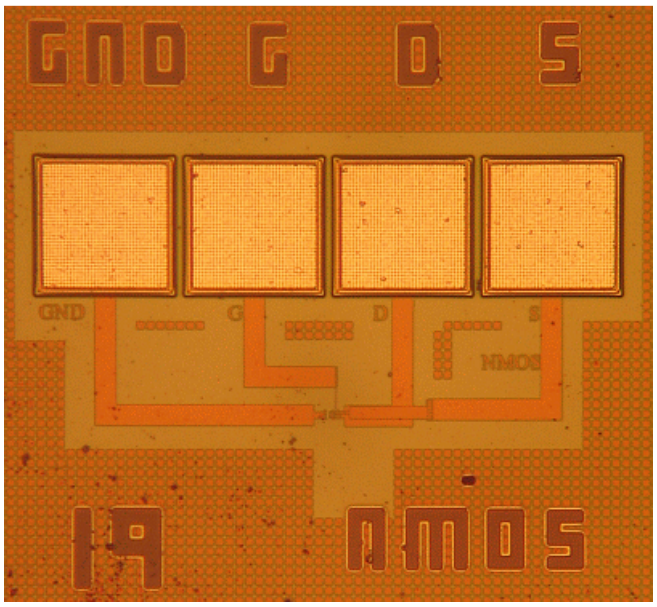


Figure 5.6 Micrograph of access transistor.

The fabricated chips were tested for any effects due to the processing steps at Idaho Micro fabrication Lab on the transistors. Simple I_D Vs V_{DS} sweeps were performed prior to and post processing steps at Boise State University. The test setup consists of the unit under test, a probe station, HP 4145 parameter analyzer and voltage supply. Figure 5.7 shows the results of sweeping the transistor's drain to source voltage from 0 to 5 V and measuring the current flowing through it. From the figure, the transistors behavior appears unchanged by the processing steps.

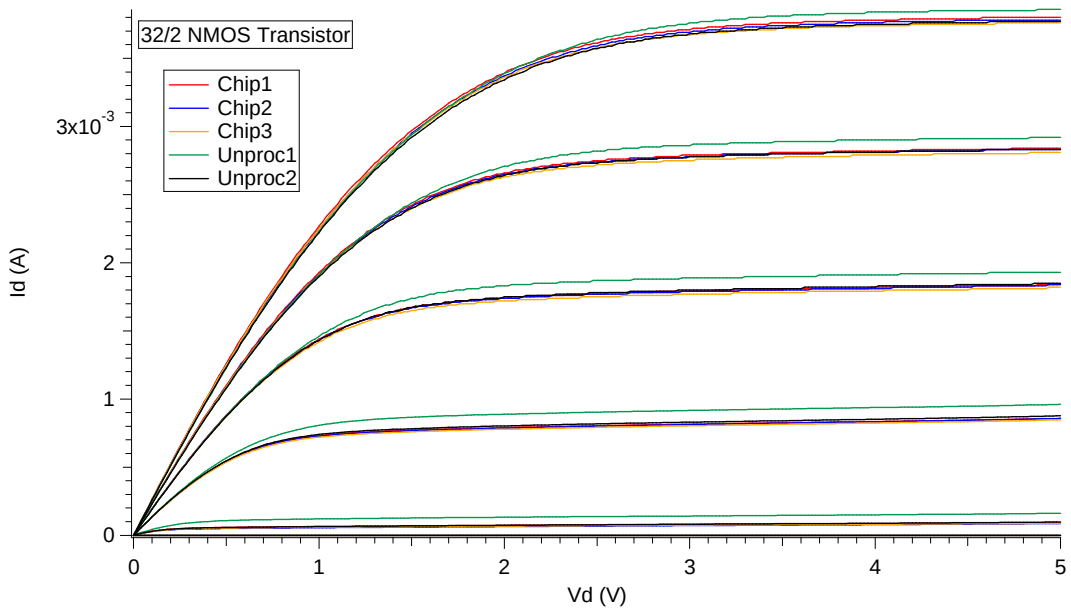


Figure 5.7 I_D vs V_{DS} curve for 32/2 NMOS access transistor.

The next sequences of test were performed on the single bit to characterize the phase change device and the resistor bit. The phase change material was characterized by forcing a current through one of the two terminal resistor bit test structure and measuring the voltage drop across the device using the HP 4145 parameter analyzer. During the post processing of the chips at IML, control wafers with tungsten bottom and top electrode were also processed along with the NASA chip with the same stack of chalcogenide for characterization. Figures 5.8 and 5.9 show two snap back regions for a positive sweep on the memory bits on the control wafers. This indicates possible multi state operation. On the resistor bits on the chip, a negative sweep was performed on the top electrode and a snap back region is noticed with two different bottom electrode sizes in Figures 5.10 and 5.11. This shows the material's phase change behavior even when the potential is reversed. This is described in more detail by Campbell et al. [5]

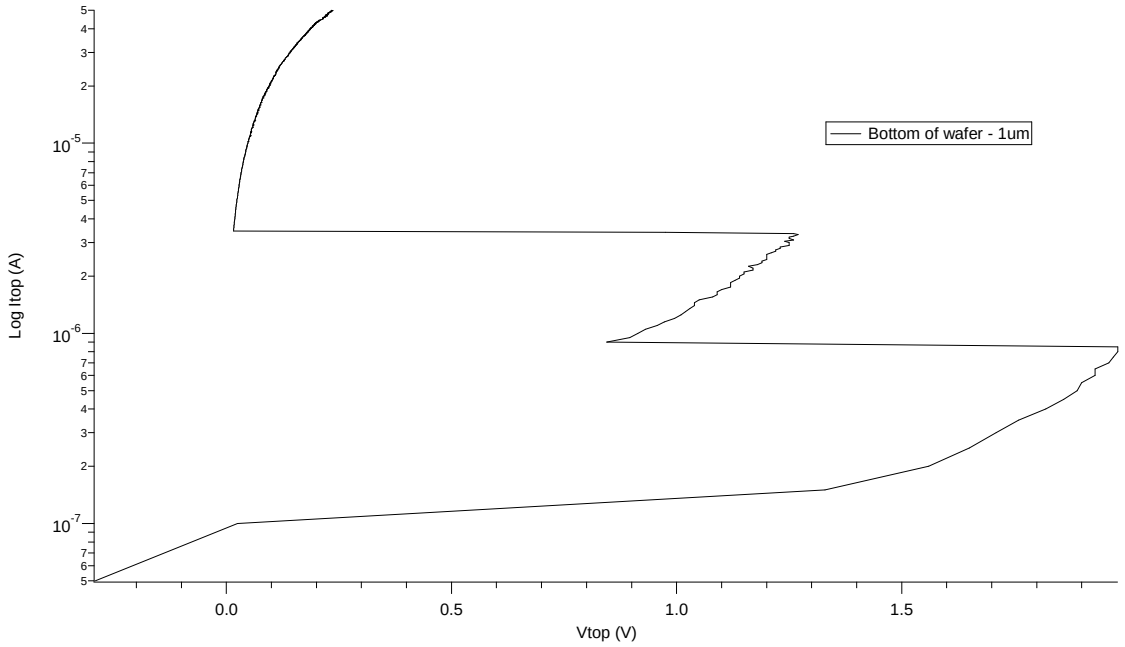


Figure 5.8 IV curve from control wafer with a stack of Ge2Se3 – SnTe. Positive sweep on top electrode (0 to 50uA, 50nA step size).

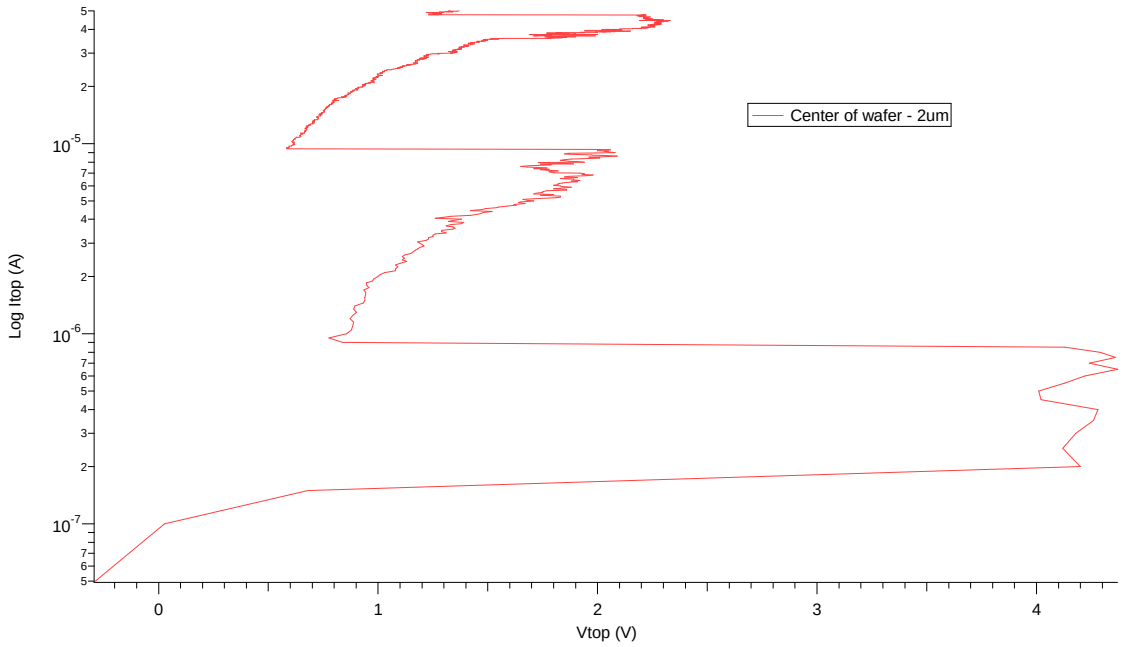


Figure 5.9 IV curve from control wafer with a stack of Ge2Se3 – SnSe. Positive sweep on top electrode (0 to 50uA, 50nA step size).

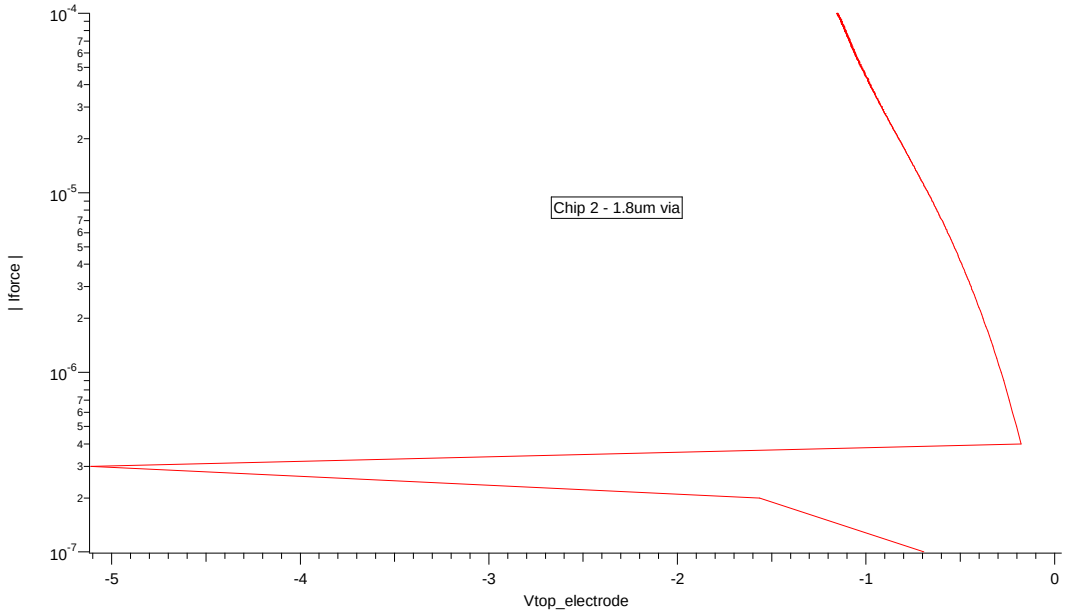


Figure 5.10 IV curve from resistor bit with a stack of Ge2Se3 – SnTe. Bottom electrode size of 1.8 µm by 1.8 µm and negative sweep on top electrode (0 to 100uA, 100nA step size).

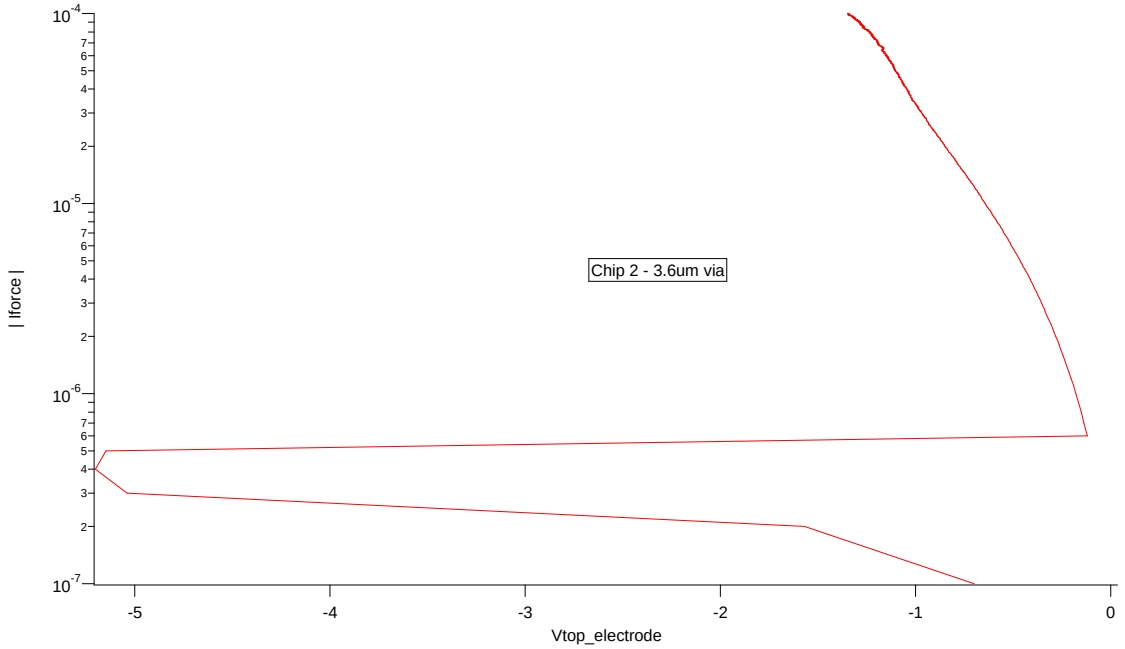


Figure 5.11 IV curve from resistor bit with a stack of Ge2Se3 – SnTe. Bottom electrode size of 3.6 µm by 3.6 µm and negative sweep on top electrode (0 to 100uA, 100nA step size).

NASA Chip 2

The second chip designed under the NASA EPSCOR project differs from the NASA chip 1 to accommodate the various limitations of the processing equipment at Idaho Microfabrication Lab. To accommodate an increased tolerance to misalignment, the number of test structures was reduced and the space between adjacent test structures and the bond pads were increased. This can be seen from the layout image shown in Figure 5.12. Also the bottom electrodes for the memory bit were fabricated using Copper in the first chip and this was replaced with Tungsten in the second chip to follow the research techniques as described by Campbell and Anderson [5]. Passivation openings were also placed on the alignment marks to provide a 3-D topographical view for better alignment.

The following information gives more details about the NASA Chip 2. Table 5.2 gives further details about the site numbers and information about the test structures.

- **Fabrication Service**: MOSIS & Idaho Micro Fabrication Lab (BSU)
- **Process**: AMI C5N
- **Design Rules**: SCMOS_SUBM
- **Lambda**: 0.30
- **Feature size**: 0.60
- **No. of Layers of Metal**: 3
- **Voltage**: 5
- **Tool**: Electric VLSI Design

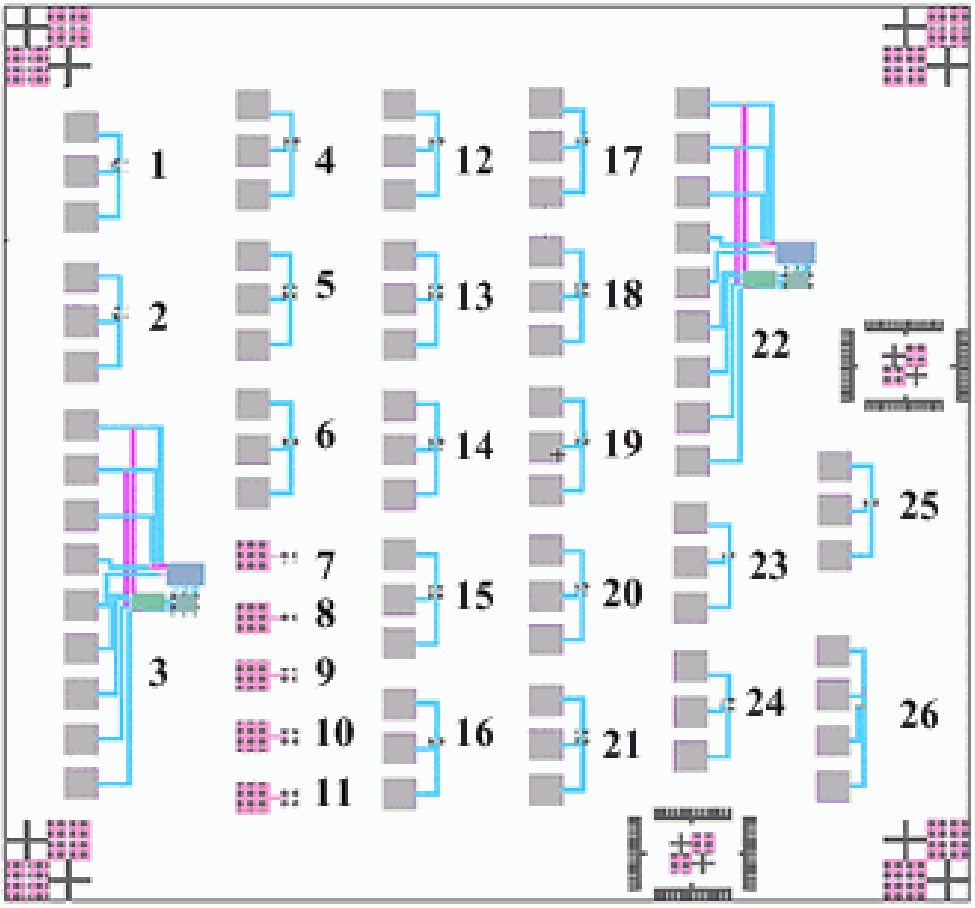


Figure 5.12 Layout view of NASA Chip 2.

Table 5.2 Description of the test structures along with their site number on the die.

Test Structure	Size	Site Location	Number of Test Structure	Comment
Array Test Structure	32/2	3, 22	2	32/2 Mbit
NMOS Bit	32/2	4, 5, 6, 12, 13, 14, 17 ,18 ,19	9	Std. Via Size (0.6 μm)
NMOS Transistor	32/2	26	1	Access Transistor
NMOS Mbit	24/2	1, 2, 25	3	Std. Via Size (0.6 μm)
NMOS Mbit	28/2	15, 20, 24	3	Std. Via Size (0.6 μm)
NMOS Mbit	40/2	16, 21, 23	3	Std. Via Size (0.6 μm)
Resistor Bit Test Structure	0.6 μm	7, 8, 9, 10, 11	5	Std. Via Size (0.6 μm)

The individual test structures on the NASA Chip 2 are shown in Figures 5.13 to 5.17. The site numbers associated with the test structures and other layout texts can be seen in the micrographs.

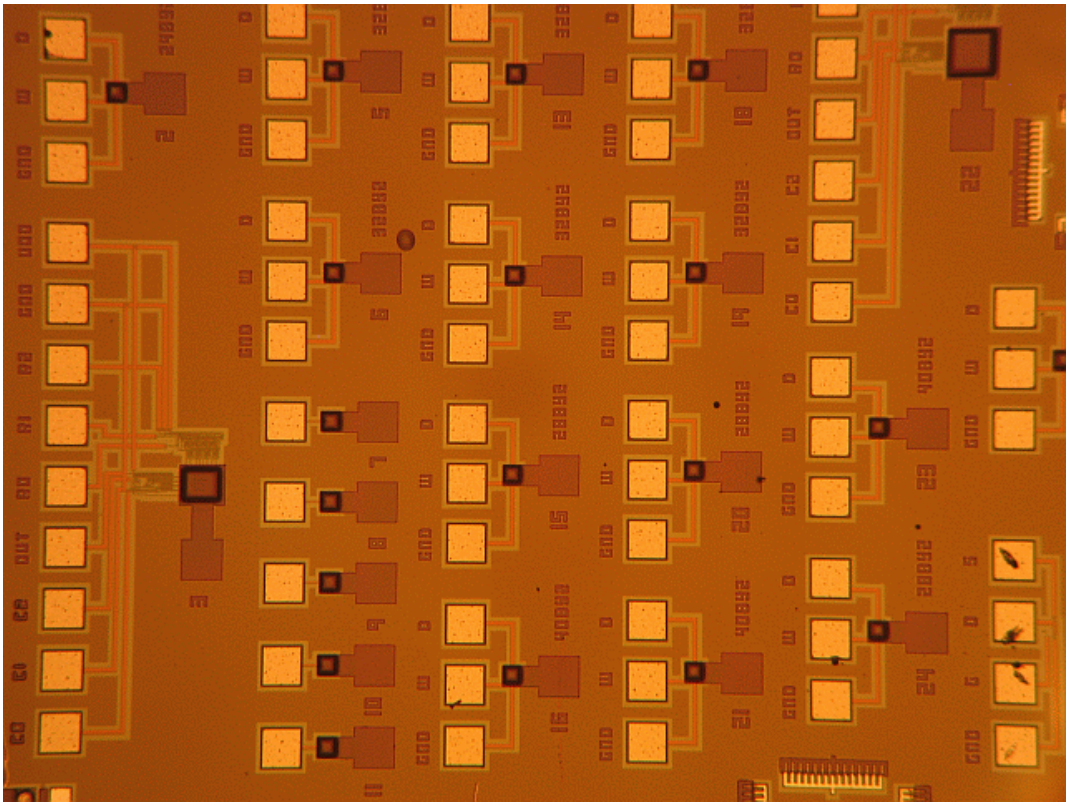


Figure 5.13 Micrograph of NASA chip 2.

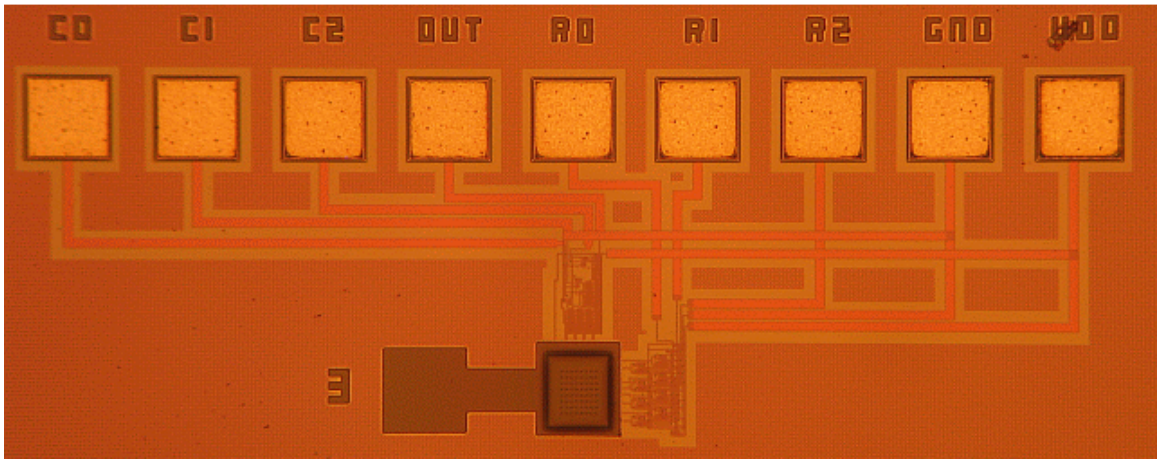


Figure 5.14 Micrograph of 64 bit memory array.

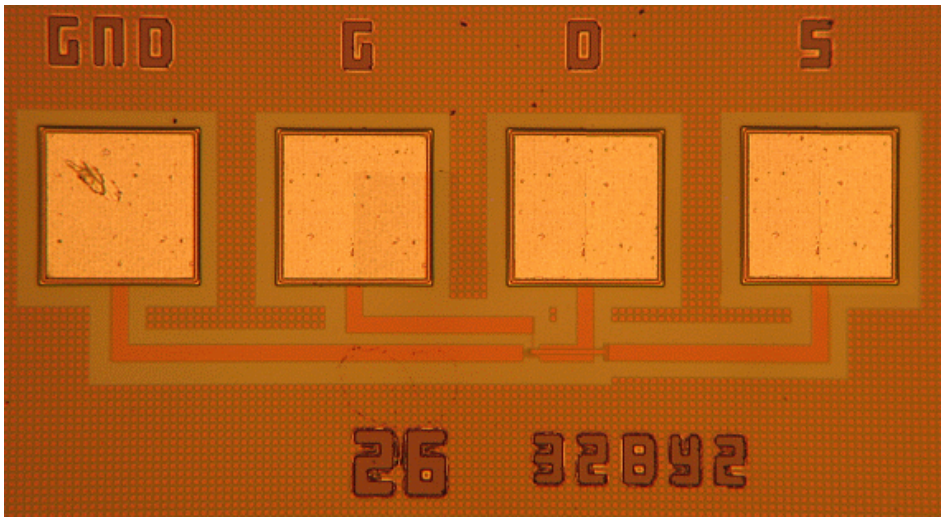


Figure 5.15 Micrograph of NMOS access transistor.

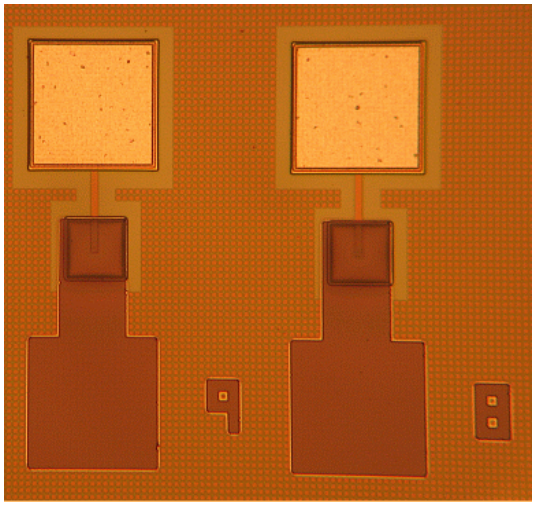


Figure 5.16 Micrograph of resistor bit.

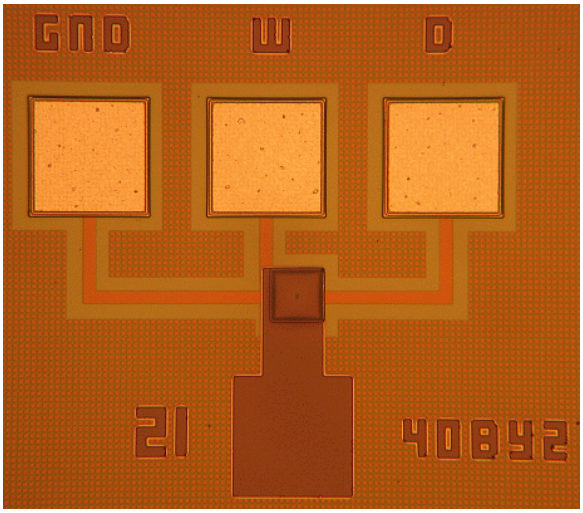


Figure 5.17 Micrograph of Mbit.

DSM Chip

The DSM chip has four variants of Delta-sigma Modulation based sensing schemes as shown in Figure 5.18. The chip micrograph is shown in Figure 5.19.

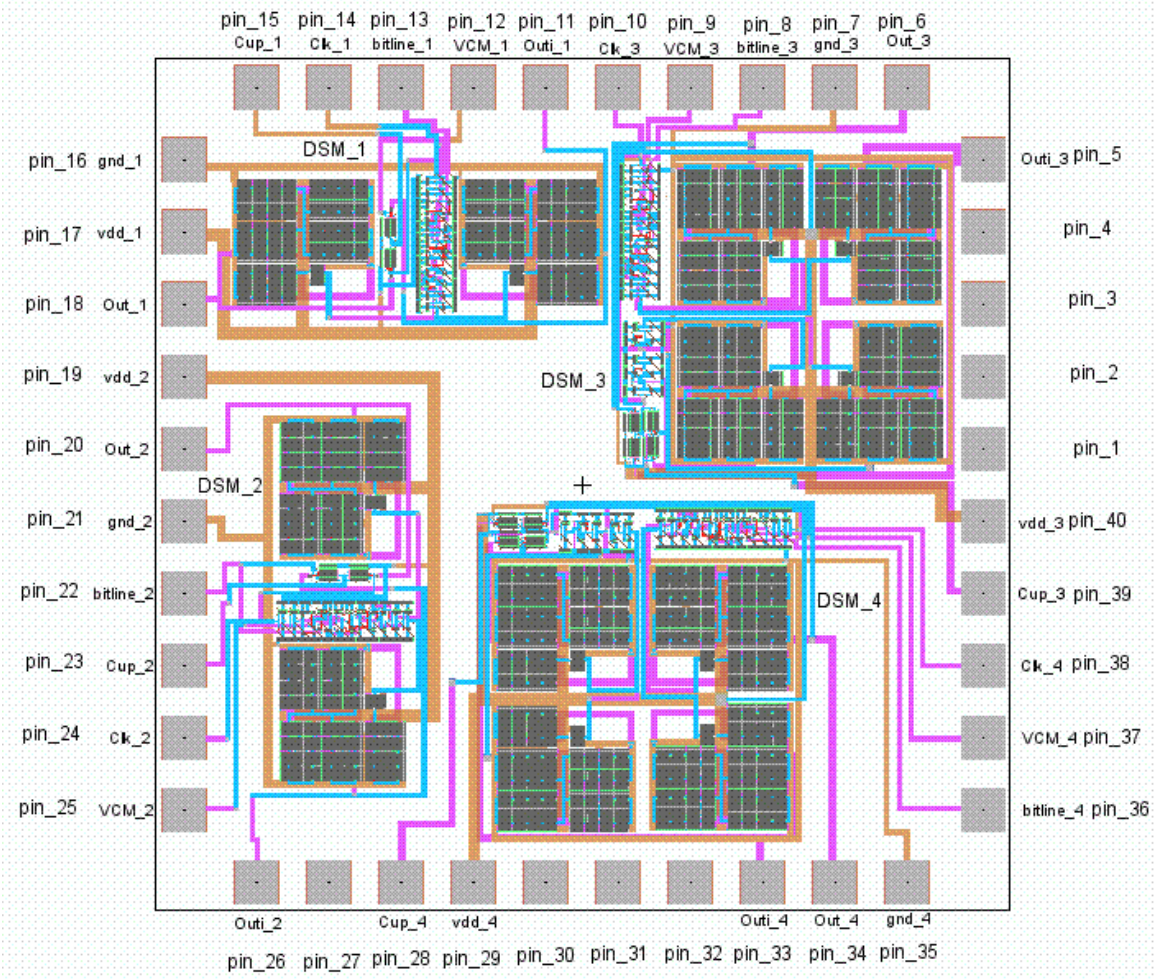


Figure 5.18 Layout view of DSM chip.

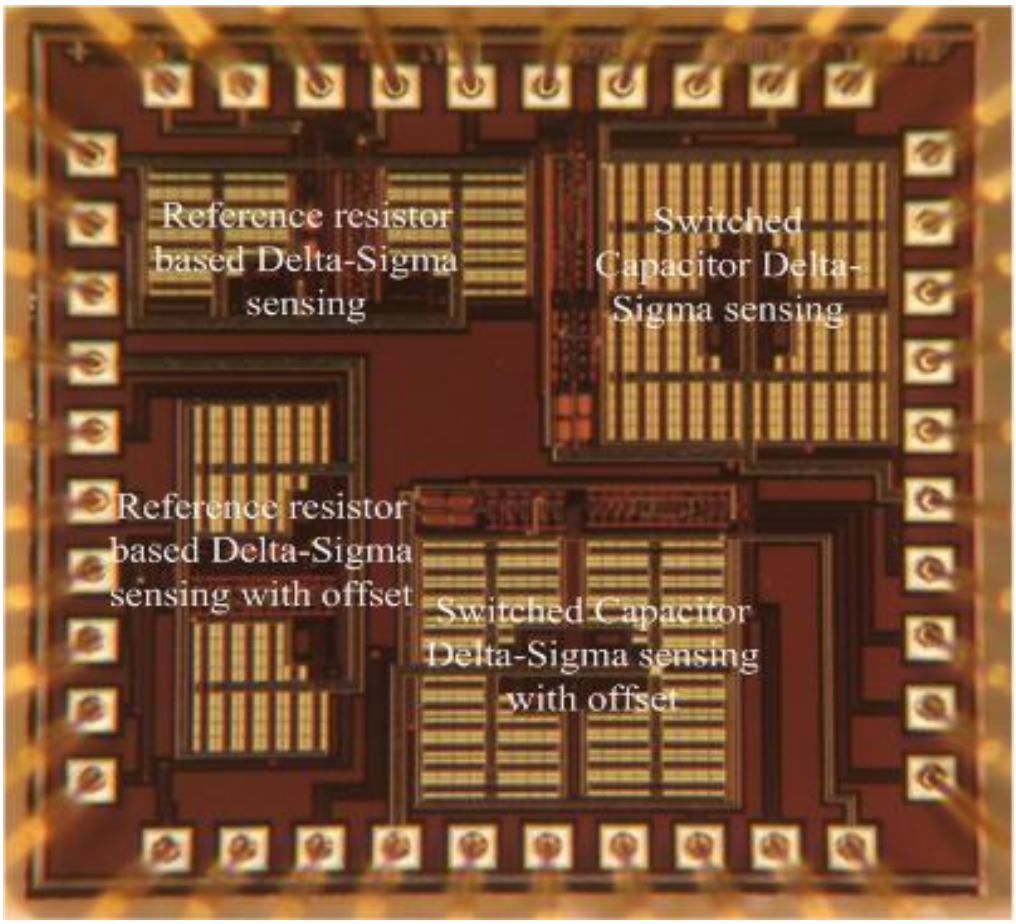


Figure 5.19 Micrograph of DSM Chip.

Figure 5.20 though 5.23 show the micrograph of the individual Delta-sigma Sense-amplifiers (DSSA). The test setup for the DSM chip is shown in Figure 5.24. The test setup consists of the unit under test, a pulse generator, dc voltage source, discrete resistance and capacitance and mixed signal oscilloscope. Figure 5.25 and 5.26 shows the DSM chip bonded into a 40 pin DIP and bread-boarded for testing.

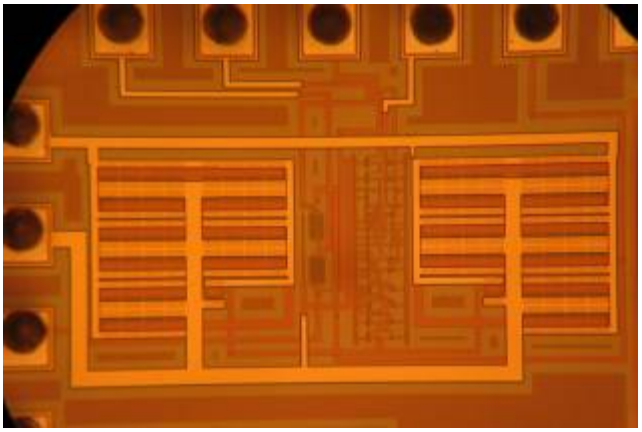


Figure 5.20 Discrete Reference resistor-based DSSA.

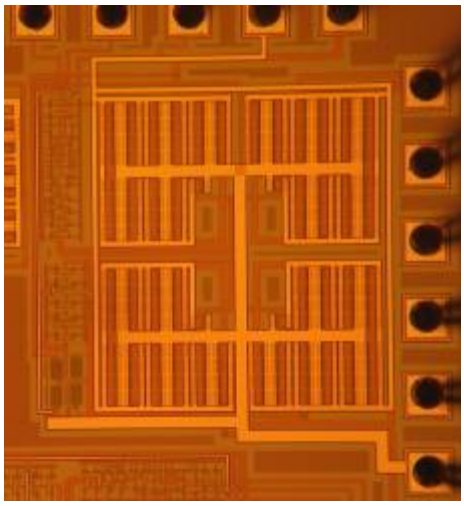


Figure 5.21 Switched-capacitor reference resistor-based DSSA.

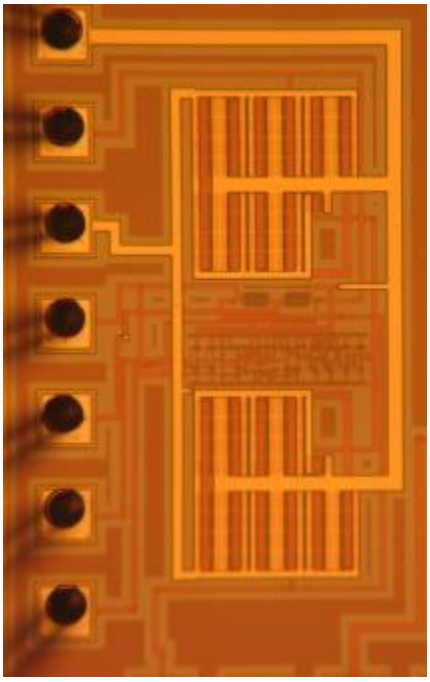


Figure 5.22 Discrete Reference resistor based DSSA with offset.

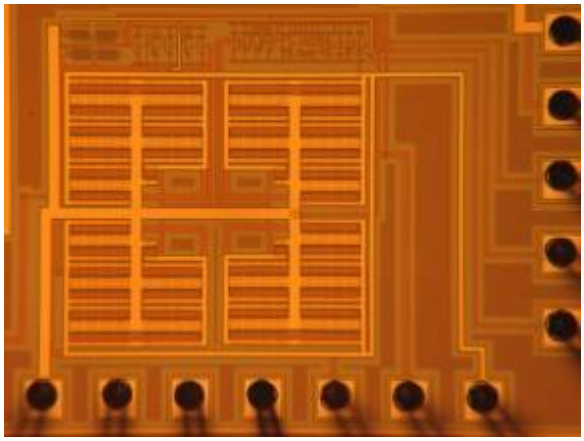


Figure 5.23 Switched-capacitor reference resistor-based DSSA with offset.

For testing purposes, a discrete resistance is connected to bitline to represent the memory bit and a discrete capacitance is added to the bitline to represent the bitline capacitance. The analog probe from the oscilloscope is connected to the bitline to see the bitline voltage variation and digital probes are connected the comparator output and clock to manually count the comparator output count (M) from the oscilloscope display. During design and calculation, the capacitances added by the analog and digital probes are taken into considerations in the formula for estimating the resistance of the memory cell.

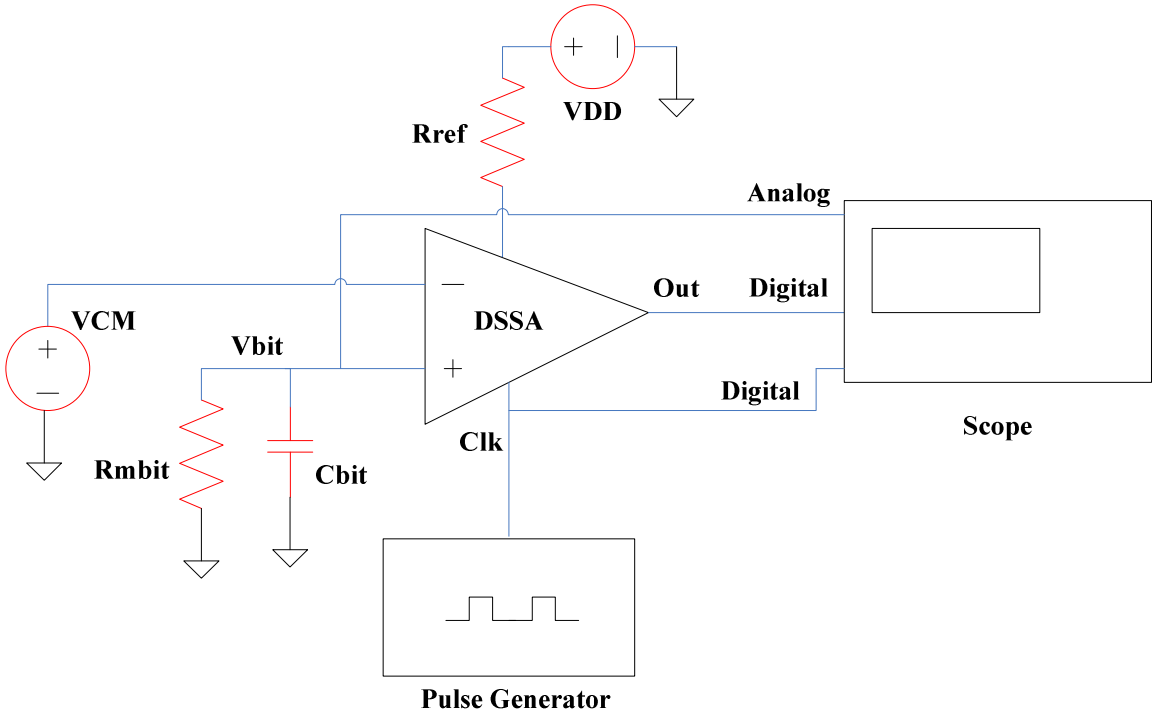


Figure 5.24 Block diagram showing the test setup for testing the DSM sense amp.

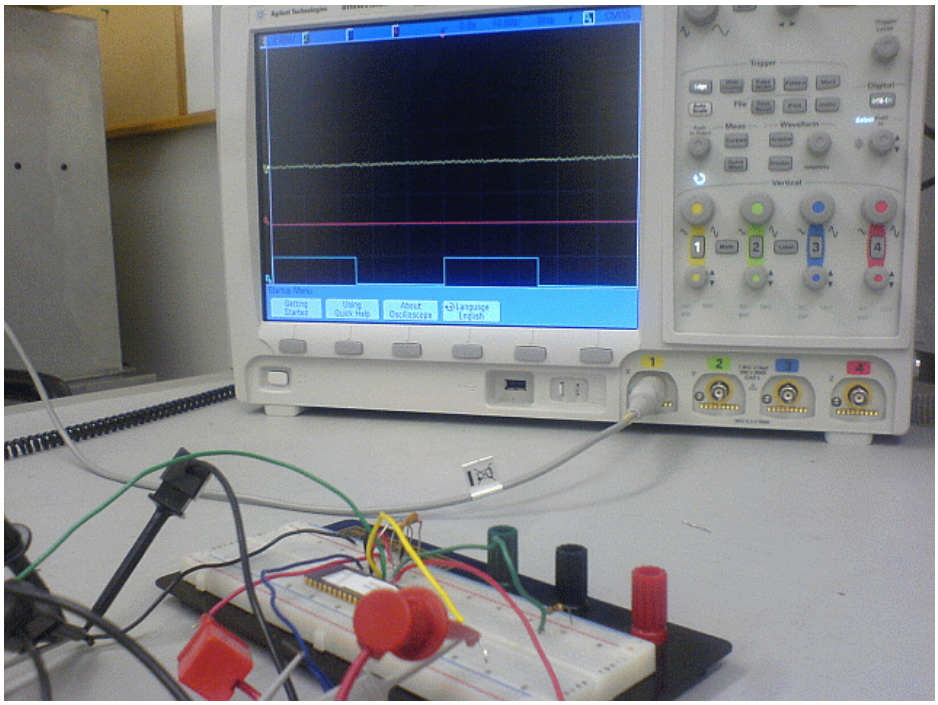


Figure 5.25 Micrograph of DSM Chip.

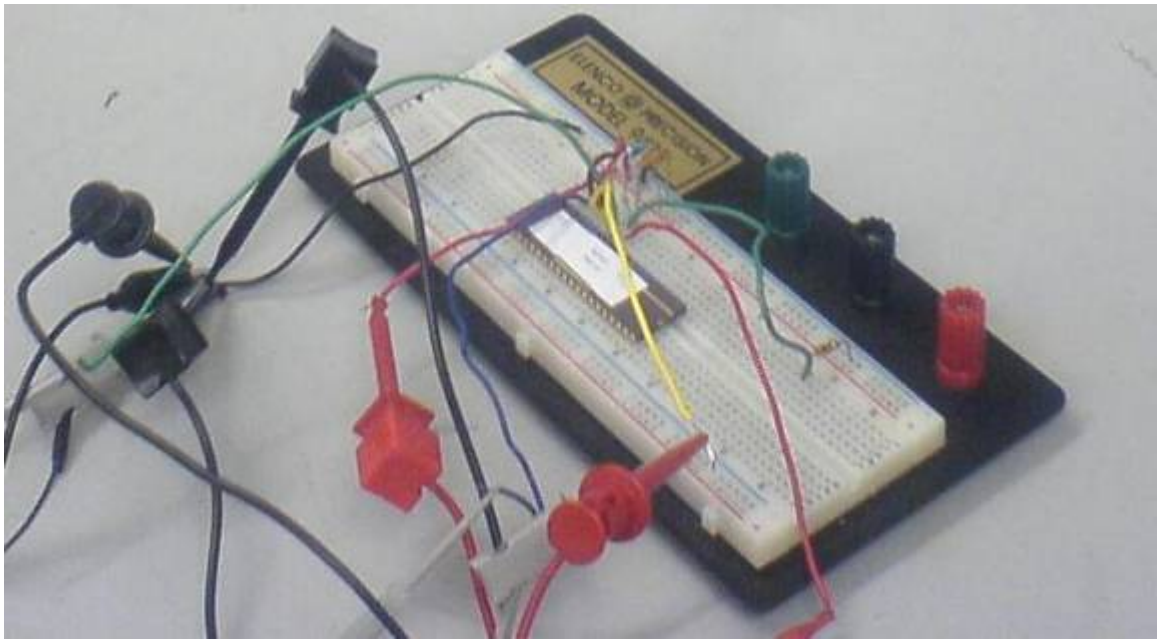


Figure 5.26 The DSM chip bonded into a 40 pin DIP and bread-boarded for testing.

A function generator is used to generate clock frequency f_{clk} = 10 MHz or f_{clk} = 15 MHz and sense time of 50 μs with N = 500 or 750 clock cycles. Note that the sense time scales with the clock frequency and the number of clock cycles. Since, due to process variations, the comparator's offset cannot be calculated accurately for two of the DSM topologies, the sensed resistance values representing the memory cells resistance are calculated by method described below. A base output count (M_{base}) is measured for a known resistor value (R_{base}). To ascertain the value for an unknown resistor (R_{sesnse}) based on output count (M_{sense}), we know that

$$R_{base} \propto 1/M_{base} \tag{1}$$

$$R_{sense} \propto 1/M_{sense} \tag{2}$$

$$R_{sense} = R_{base} \times \left(M_{base} / M_{sense} \right) \tag{3}$$

The test plots for the DSM topologies are shown in the oscilloscope screen captures in Figures 5.27 to 5.29. The performance of the four DSM sense amp variants are compared with their simulation results and are presented in the plots seen in Figures. 5.30 to 5.33. The chip test data for the plots are obtained from Table 5.3 through 5.10 and the simulation data from Table 4.2 to 4.5 in Chapter 4. The simulation results and the results from chip testing were found to match closely in all topologies with variations likely due to the assumed values for the parasitics, including the large off-chip capacitances. Also the comparator offset used in the formula for the calculation of sensed resistance from the simulation data may not actually match with the comparator offset in the fabricated chip. These parasitic capacitances and comparator offset can be estimated by including dedicated test structures in the fabricated chip and can be added to the simulations to show a near exact match between measurements and simulation. However,

since this doesn't add value to the design, or influence the final results in a practical sensing circuit, we simply point it out before presenting the test results.

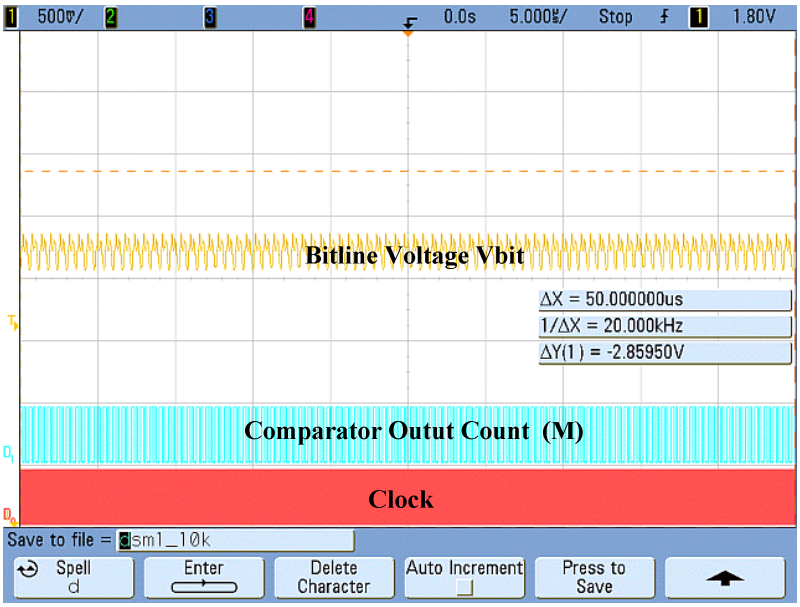


Figure 5.27 Test result for discrete reference resistor-based DSM topology with no offset for a sensed resistance of 10 kΩ.

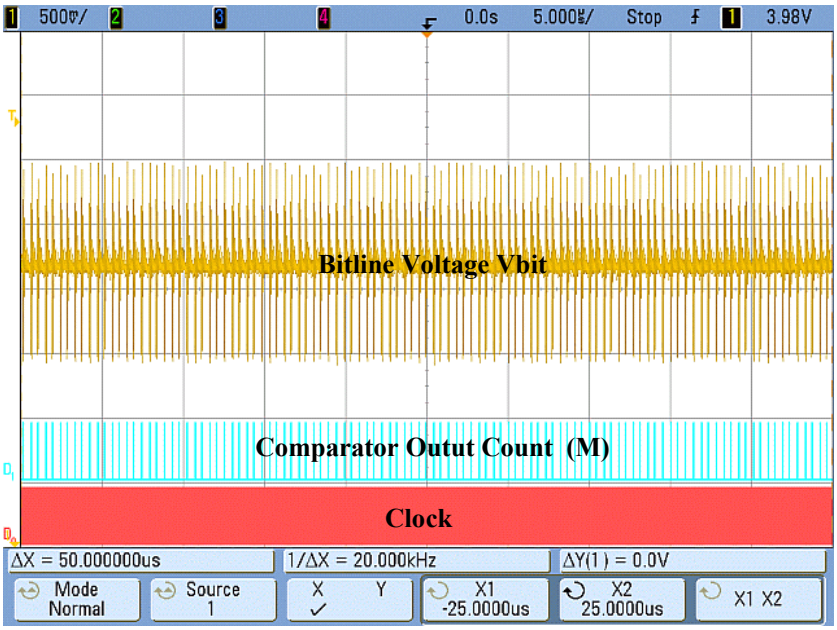


Figure 5.28 Test result for discrete reference resistor-based DSM topology with offset for a sensed resistance of 10 kΩ.

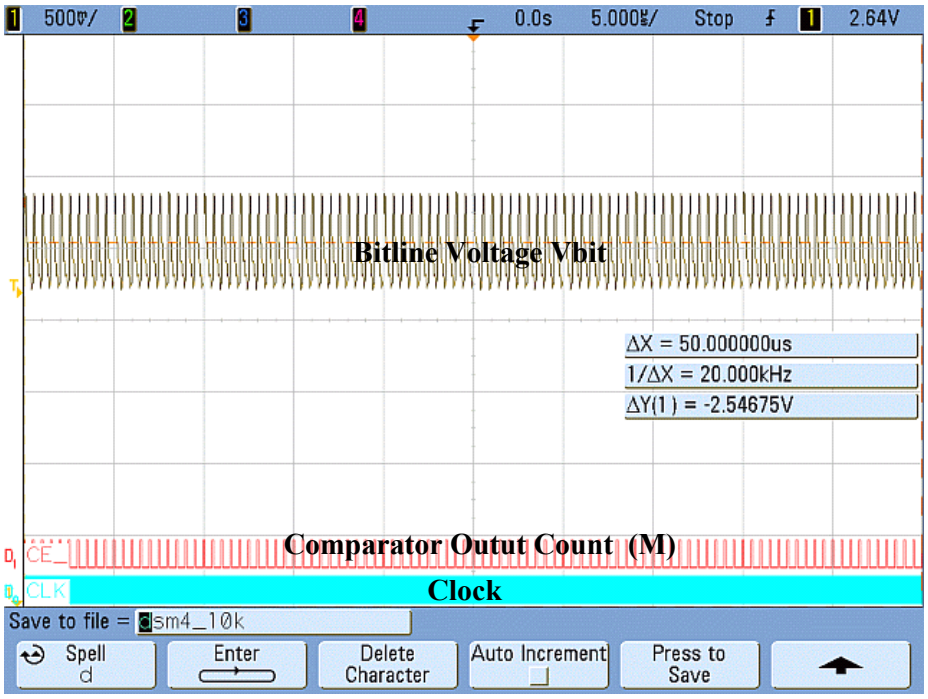


Figure 5.29 Test result for switched-capacitor reference resistor-based DSM topology with offset for a sensed resistance of 10 kΩ.

The parameter used for testing and calculating the sensed resistor using reference resistor-based ΔΣ sense amp without offset is shown in Table 5.3.

Table 5.3 Reference Resistor-based ΔΣ Sense amp without offset test details.

Clock frequency	10 MHz	**Formula Used**
Rref	5 kΩ	$Rmbit = (Rcup) * \left(\frac{N}{M}\right)$
Cref	parasitc=0.2 pF	
Cout	8 pF	
Cbit	68 pF	
Cprobe on Bitline	14 pF	
N	500 clock cycles	
Cbittotal	82 pF	

Table 5.4 Reference Resistor-based ΔΣ Sense amp without offset test results.

Resistor Actual (kΩ)	Comparator output Count M	Resistor Sensed (kΩ)
10	250	10
20	170	15
30	108	23
40	83	30
50	67	37
60	55	45
70	50	50
80	47	53
90	39	64
100	35	71
110	33	76
120	32	78
130	27	93
140	27	94
150	25	100
160	24	104
170	23	109
180	21	119
190	19	132
200	19	133

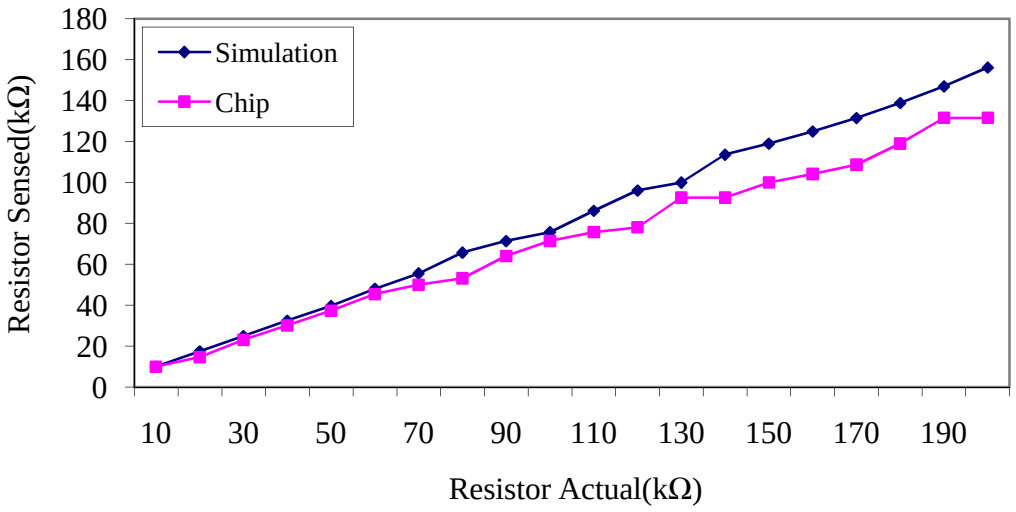


Figure 5.30 Resistor sensed vs. resistor actual for reference resistor-based Delta-Sigma Sensing.

The parameter used for testing and calculating the sensed resistor using reference resistor-based ΔΣ sense amp with offset is shown in Table 5.5.

Table 5.5 Reference Resistor-based ΔΣ Sense amp with offset test details.

Clock frequency	15 MHz	**Formula Used**
Rref	5 kΩ	$Rmbit = (Rcup) * \left(\frac{N}{M}\right) * ((Vos)/(VDD/2 - Vos))$ $Vos = 120mv$
Cout	8 pF	
Cref	parasitic=0.2 pF	
N	750 clock cycles	
Cbit	130 pF	
Cprobe on Bitline	14 pF	
Cbittotal	144 pF	

Table 5.6 Reference Resistor-based ΔΣ Sense amp with offset test results.

Resistor Actual (kΩ)	**Comparator output Count M**	**Resistor Sensed (Using equation) (kΩ)**	**Resistor Sensed (Using ratios) (kΩ)**
10	44	3	5
20	26	5	8
30	15	8	15
40	14	9	16
50	12	11	18
60	11	11	20
70	10	13	22
80	9	14	24
90	7	18	31
100	6	21	37
110	5	25	44
120	5	25	44
130	4	32	55
140	3	42	73
150	3	42	73
160	2	63	110
170	2	63	110
180	1	126	220
190	1	126	220

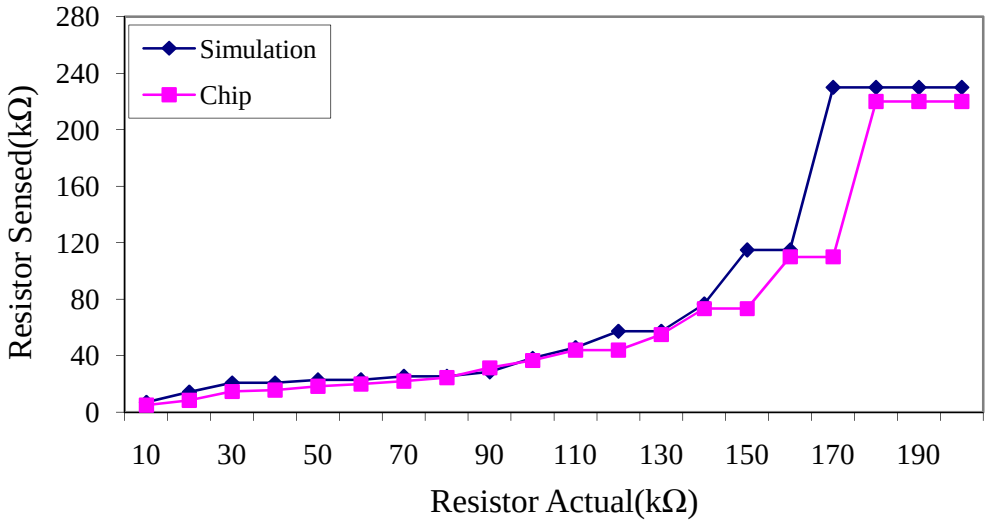


Figure 5.31 Resistor sensed vs. resistor actual for reference resistor-based Delta-Sigma Sensing with offset.

The parameter used for testing and calculating the sensed resistor using switched-capacitor resistor-based ΔΣ sense amp without offset is shown in Table 5.7.

Table 5.7 Switched-capacitor resistor-based ΔΣ sense amp without offset test details.

Clock frequency	10 MHz	**Formula Used**
Rsc(switched cap res)	27.77 kΩ	$Rmbit = (Rsc) * \left(\frac{N}{M}\right)$
Cout	8 pF	
Ccup	3.6 pF	
N	500 clock cycles	
Cbit	3.6 pF	
Cprobe on Bitline	14 pF	
Cbittotal	17.6 pF	

Table 5.8 Switched-capacitor resistor-based ΔΣ sense amp without offset test results.

Resistor Actual (kΩ)	Comparator Output Count M	Resistor Sensed (kΩ)
108	123	113
147	90	154
205	67	207
248	55	253
298	47	296
350	43	323
403	37	375
458	33	421
497	31	448
560	22	631
620	20	694
1000	15	926
1500	10	1389
2400	9	1543
4100	6	2315

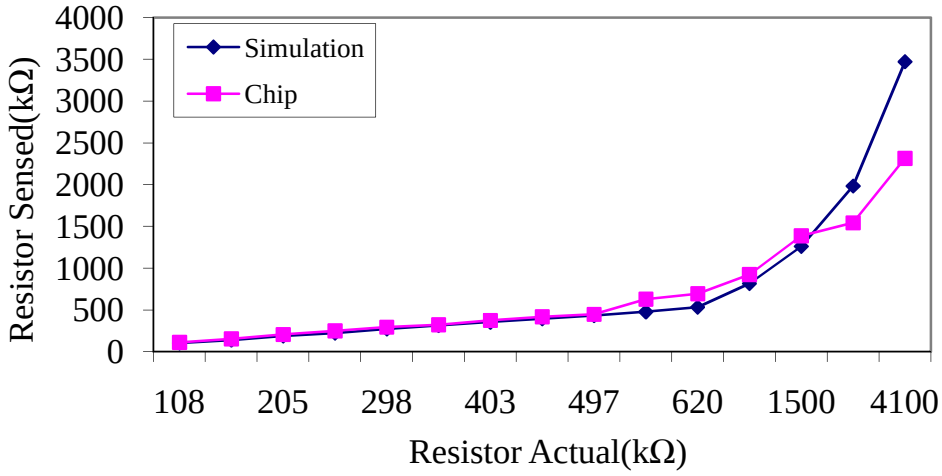


Figure 5.32 Resistor sensed vs. resistor actual for switched-capacitor resistor-based Delta-Sigma sensing.

The parameter used for testing and calculating the sensed resistor using switched-capacitor resistor-based ΔΣ sense amp with offset is shown in Table 5.9.

Table 5.9 Switched-capacitor resistor-based ΔΣ sense amp with offset test details.

Clock frequency	10 MHz	**Formula Used**
Rsc(switched cap res)	27.77 kΩ	$Rmbit = (Rsc) * \left(\frac{N}{M}\right) * ((Vos) / (VDD / 2 - Vos))$
Cout	8 pF	
Ccup	3.6 pF	
N	500 clock cycles	
Cbit	3.6 pF	
Cprobe on Bitline	14 pF	
Cbittotal	17.6 pF	

Table 5.10 Switched-capacitor resistor-based ΔΣ sense amp with offset test results.

Resistor Actual (kΩ)	**Comparator Output Count M**	**Resistor Sensed (Using equation) (kΩ)**	**Resistor Sensed (Using ratios) (kΩ)**
10	100	7	10
20	55	13	18
30	39	18	26
40	31	23	32
50	27	26	37
60	23	30	43
70	19	37	53
80	17	41	59
90	16	44	63
100	14	50	71
110	13	54	77
120	13	54	77
130	11	64	91
140	11	64	91
150	10	70	100
160	10	70	100
170	9	78	111
180	9	78	111
190	8	88	125
200	8	88	125

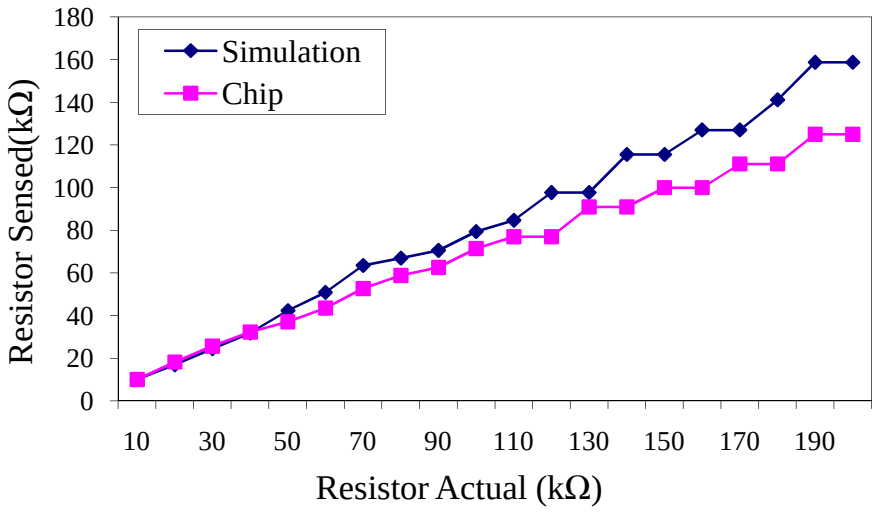


Figure 5.33 Resistor sensed vs. resistor actual for switched-capacitor resistor-based Delta-Sigma sensing with offset.

The test results of the four DSSA are compared in Table 5.11. The results reiterate the flexibility and accuracy of all four topologies. Even though the parasitic capacitances and the comparator offset weren't estimated accurately, the error percentage of all four topologies with respect to the simulation result was found to be in minimal and in the range of 10 to 15 %. This error percentage is very acceptable in resistive memory sensing were the resistances of SET and RESET states usually vary from a few kΩ to several MΩ [5], [21], [22]. These encouraging test results warrant further tests in conjunction with phase change devices to study performance and implementation of Delta-sigma Sensing techniques.

Table 5.11 Comparison of four DSSA topologies.

Topology Name	f_{clk}	**Sense time**	**Range of resistance**	**% error**
Reference resistor-based DSSA	10 MHz	50 μs	10 – 200 kΩ	11.7 %
Reference resistor-based DSSA with offset	15 MHz	50 μs	10 – 200 kΩ	15.7 %
Switched-capacitor resistor-based DSSA	10 MHz	50 μs	0.1 – 4.1 MΩ	13.7 %
Switched-capacitor resistor-based DSSA with offset	10 MHz	50 μs	10 – 200 kΩ	15.2 %

CONCLUSIONS

This thesis presents results from integrating two discreet processing services to fabricate chalcogenide based phase change non volatile memory. Several creative and innovative ideas were employed in the design and layout of PCM chips to overcome the obstacles of integrating the MOSIS fabrication service with the processing equipments available at IML. The test results from chalcogenide based resistor bits indicate potential multi state operation and hence the possibility to store multiple bits on a single memory devices. The access transistors were tested for any effects due to the post processing steps and none were found. These tests indicate the successful integration of a commercially available CMOS process with in house processing with exotic materials for research and development of new devices and memory technologies.

The second part of the dissertation presents novel Delta-sigma based sensing techniques to sense the state of chalcogenide based resistive memory. The four DSM topologies illustrate the flexibility of the sensing techniques by employing a combination of discreet resistors or switched-capacitor resistors and comparator with or without offset with a mere 10 to 15% error margin. These error margins can be attributed to large off chip capacitance at the reference resistor, memory resistor and sigma capacitor terminals. If these components were developed on chip, the projected sense time would decrease from 50 μs to 5 μs with error percentage remaining almost same. With the separation between two adjacent states being more than 100% in most cases [5], [23], this result

exceeds the performance required by sense-amplifiers for resistive memory sensing. The sense-amplifiers designed were also robust enough to sense a wide range resistance from 10 kΩ to 4.1 MΩ with same accuracy.

Future design revision would focus on increasing the performance and reducing the power consumption of the DSSA. One way of achieving this would be to include the reference resistor and the bitline capacitance on chip to reduce the effect of capacitive loading from the bond pads. Scaling down the technology used to fabricate the chip is another way of improving the speed and reducing the power and layout area.

The DSM based sense-amplifiers designed have the flexibility to increase the accuracy by increasing the sense time. The comparator and its clock can also be optimized to improve the precision of the sense-amplifier. The sense time can be reduced if high precision is not required during the sensing operation.

The DSM based sense-amplifier presented in this thesis is to prove the concept of Delta-sigma Modulation in sensing applications for resistive memory. Applying additional creativity in design and using latest technology in future designs could prove the competitiveness of DSM based sensing circuits in sensing resistive memories.

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